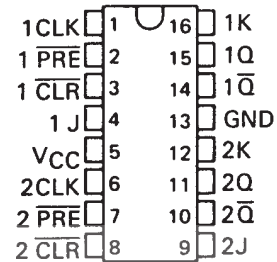# SN5476, SN54LS76A
SN7476, SN74LS76A
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages**

- **Dependable Texas Instruments Quality and Reliability**

description

The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flip-flop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predicatble operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7476 and the SN74LS76A are characterized for operation from 0°C to 70°C.

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)

```
1CLK   [ 1    16 ]  1K
1 PRE  [ 2    15 ]  1Q
1 CLR  [ 3    14 ]  1Q̄
1 J    [ 4    13 ]  GND
VCC    [ 5    12 ]  2K
2CLK   [ 6    11 ]  2Q
2 PRE  [ 7    10 ]  2Q̄
2 CLR  [ 8     9 ]  2J
```

'76 FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⎍	L	L	Q_0	$\overline{Q_0}$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

'LS76A FUNCTION TABLE

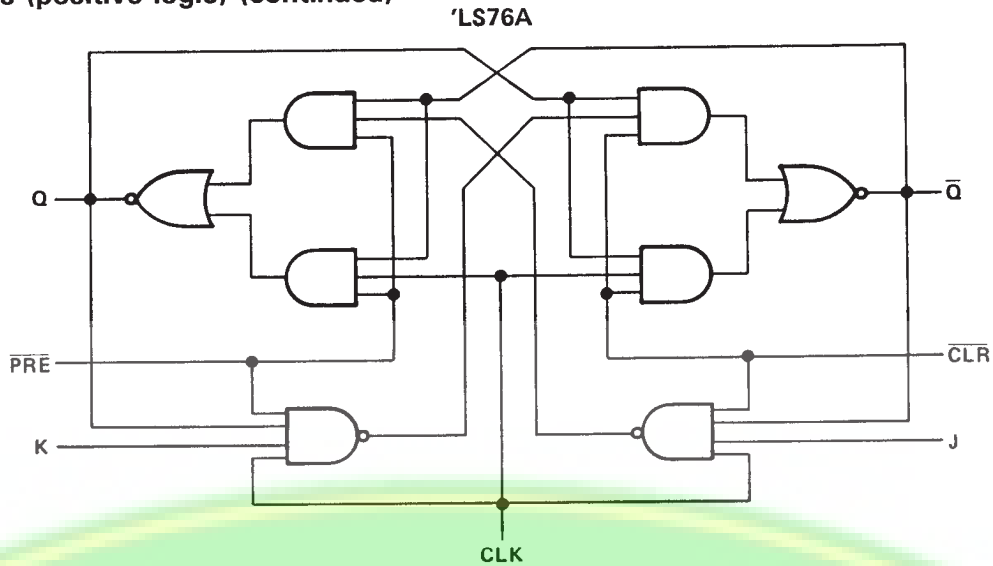| INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q_0}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q_0}$

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

Copyright © 1988, Texas Instruments Incorporated

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

1

logic diagrams (positive logic)

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265
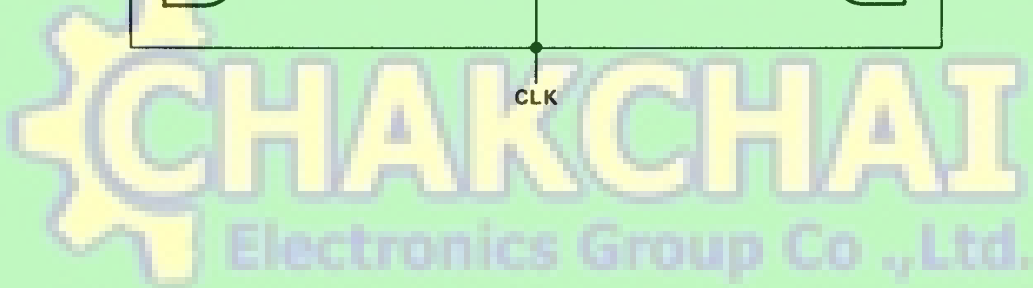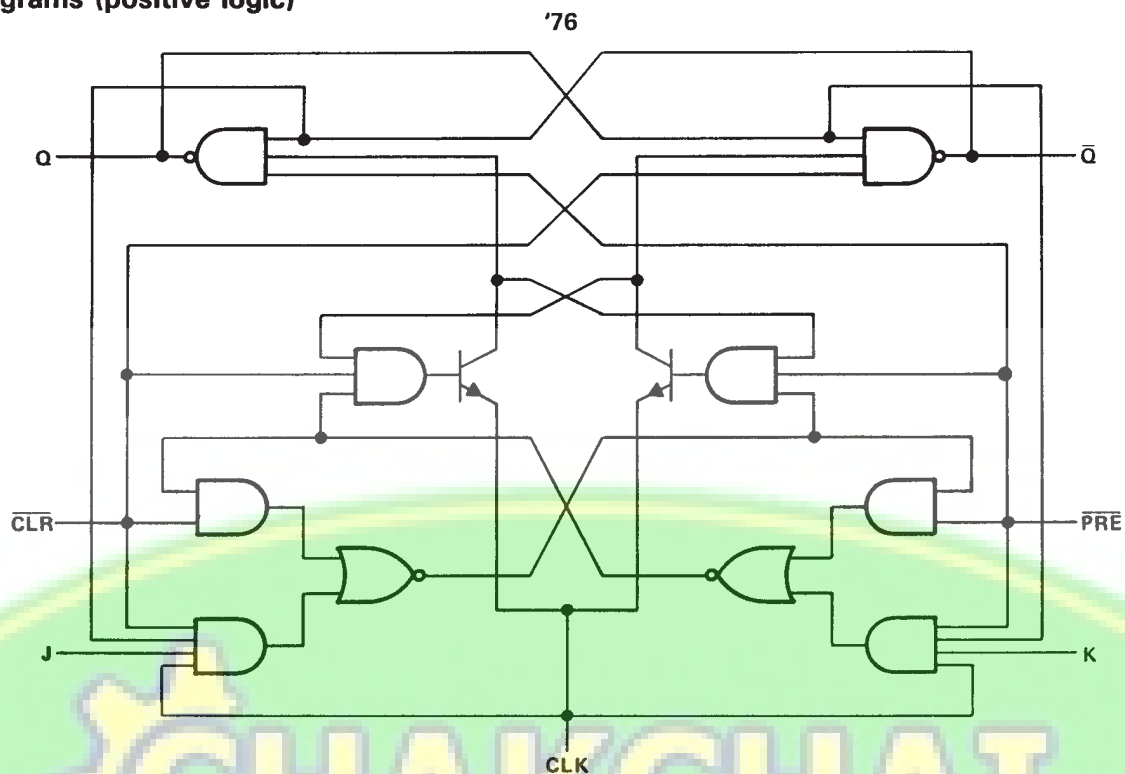
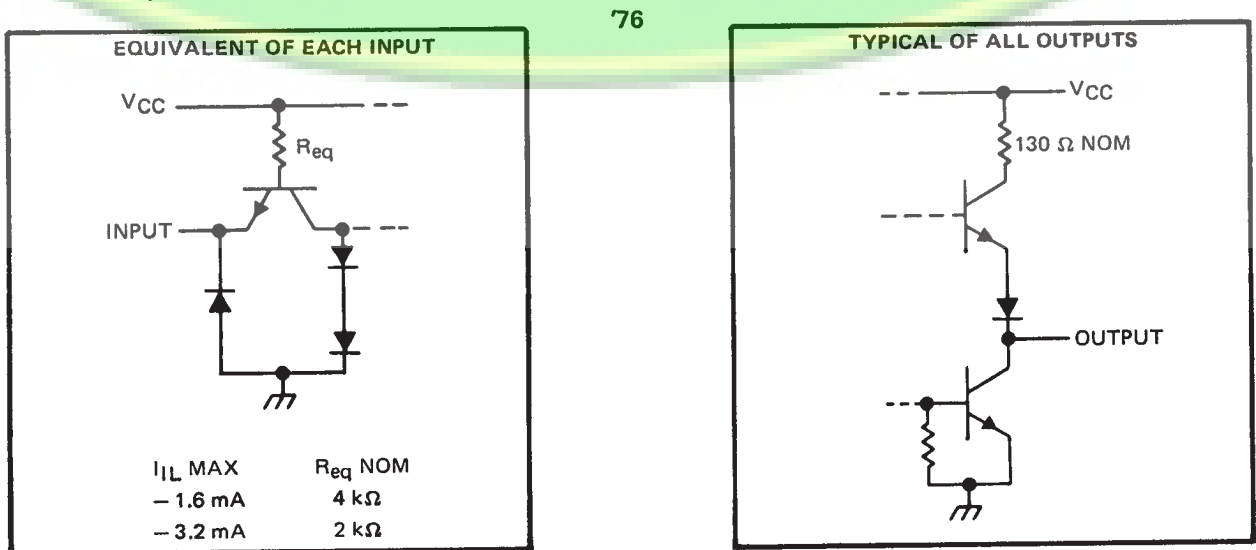## logic diagrams (positive logic) (continued)

'LS76A

logic symbols[†]
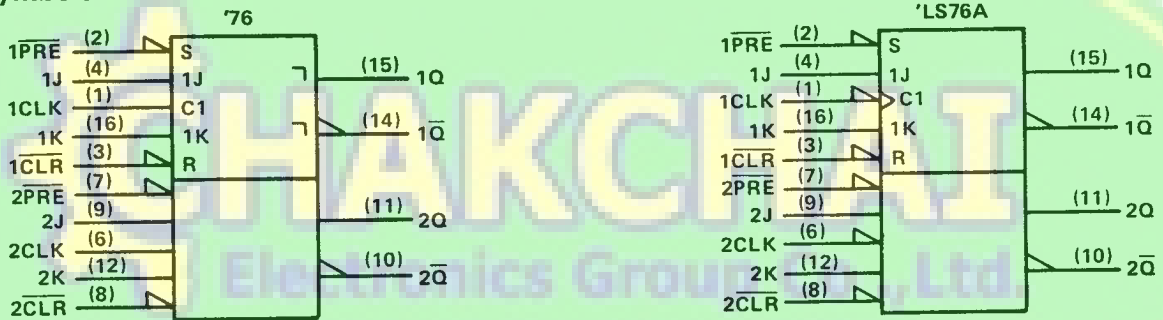
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
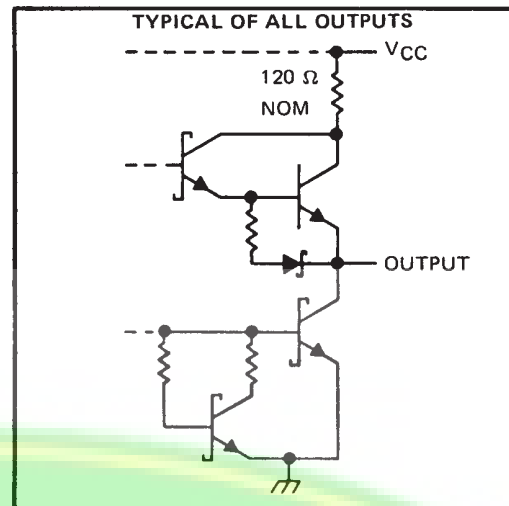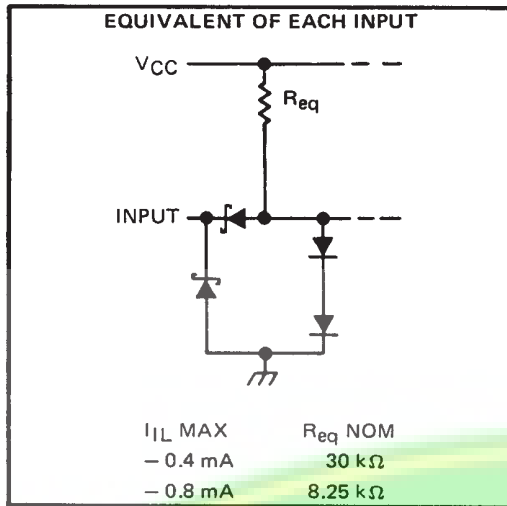
schematics of inputs and outputs

'76

I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−3.2 mA	2 kΩ

130 Ω NOM

schematics of inputs and outputs (continued)

'LS76A

EQUIVALENT OF EACH INPUT

I_{IL} MAX	R_{eq} NOM
− 0.4 mA	30 kΩ
− 0.8 mA	8.25 kΩ

TYPICAL OF ALL OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: '76 . . . . 5.5 V
              'LS76A . . . . 7 V
Operating free-air temperature range: SN54' . . . . − 55°C to 125°C
                              SN74' . . . . 0°C to 70°C
Storage temperature range . . . . − 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.
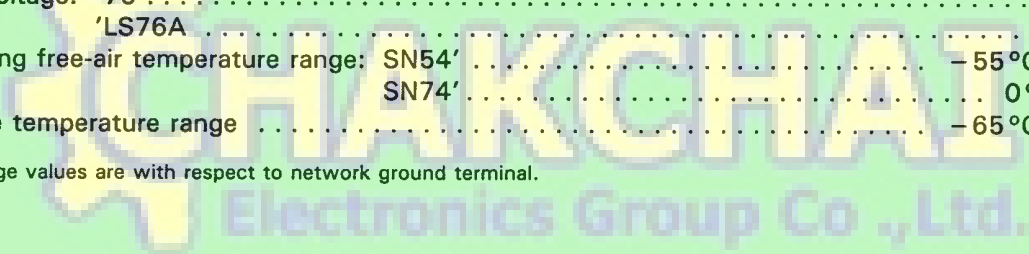
TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions

			SN5476			SN7476			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				– 0.4			– 0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	20			20			ns
		CLK low	47			47			
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Input setup time before CLK ↑		0			0			ns
t_h	Input hold time-data after CLK ↓		0			0			ns
T_A	Operating free-air temperature		– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN5476			SN7476			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = – 12 mA			– 1.5			– 1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = – 0.4 mA		2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
	All other					80			80	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V			– 1.6			– 1.6	mA
	All other[¶]					– 3.2			– 3.2	
I_{OS}[§]		V_{CC} = MAX		– 20		– 57	– 18		– 57	mA
I_{CC}[#]		V_{CC} = MAX,	See Note 2		10	20		10	20	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time.
[¶] Clear is tested with preset high and preset is tested with clear high.
[#] Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}					15	20		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	R_L = 400 Ω,	C_L = 15 pF		16	25	ns
t_{PHL}						25	40	ns
t_{PLH}	CLK	Q or $\overline{Q}$				16	25	ns
t_{PHL}						25	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5476, SN54LS76A
SN7476, SN74LS76A
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

			SN54LS76A			SN74LS76A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				− 0.4			− 0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		$\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time before CLK↓	data high or low	20			20			ns
		$\overline{CLR}$ inactive	20			20			
		$\overline{PRE}$ inactive	25			25			
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS76A			SN74LS76A			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = − 18 mA			− 1.5			− 1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = − 0.4 mA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 4 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 8 mA						0.35	0.5	
I_I	J or K					0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$	V_{CC} = MAX,	V_I = 7 V			0.3			0.3	
	CLK					0.4			0.4	
I_{IH}	J or K					20			20	µA
	$\overline{CLR}$ or $\overline{PRE}$	V_{CC} = MAX,	V_I = 2.7 V			60			60	
	CLK					80			80	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V			− 0.4			− 0.4	mA
	All other					− 0.8			− 0.8	
I_{OS}[§]		V_{CC} = MAX,	See Note 4	− 20		− 100	− 20		− 100	mA
I_{CC} (Total)		V_{CC} = MAX,	See Note 2		4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ,	C_L = 15 pF	30	45		MHz
t_{PLH}	$\overline{PRE}$, $\overline{CLR}$ or CLK	Q or $\overline{Q}$				15	20	ns
t_{PHL}						15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9557501QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9557501QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9557501QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
7601301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
7601301EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/00204BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
JM38510/00204BEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN5476J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN5476J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN7476N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN7476N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN7476N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN7476N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS76AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS76AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS76ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS76ADR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS76AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS76AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS76AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS76AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ5476J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ5476J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ5476W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ5476W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS76AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS76AW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS76AW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
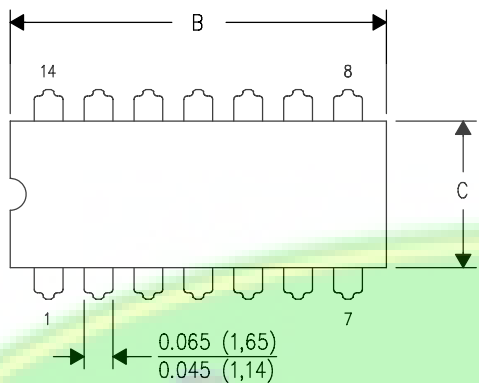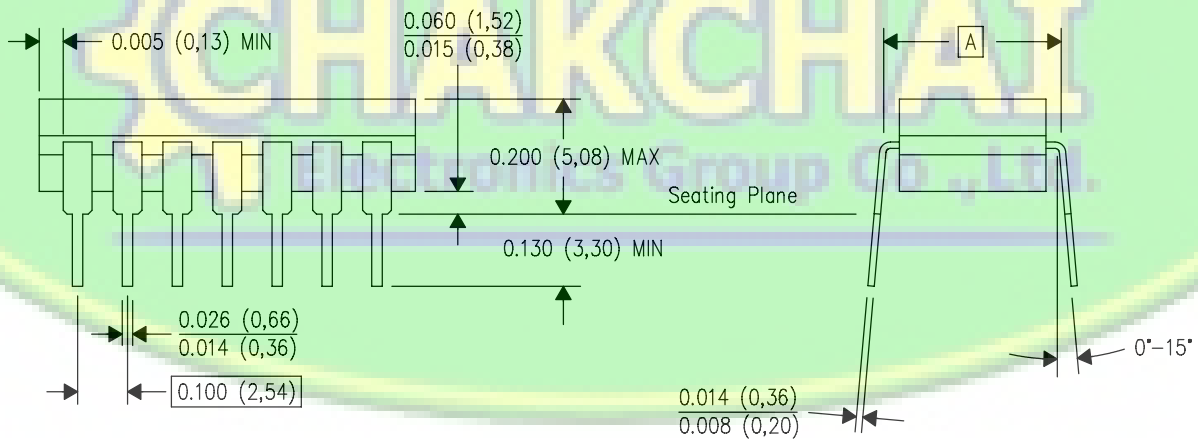
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

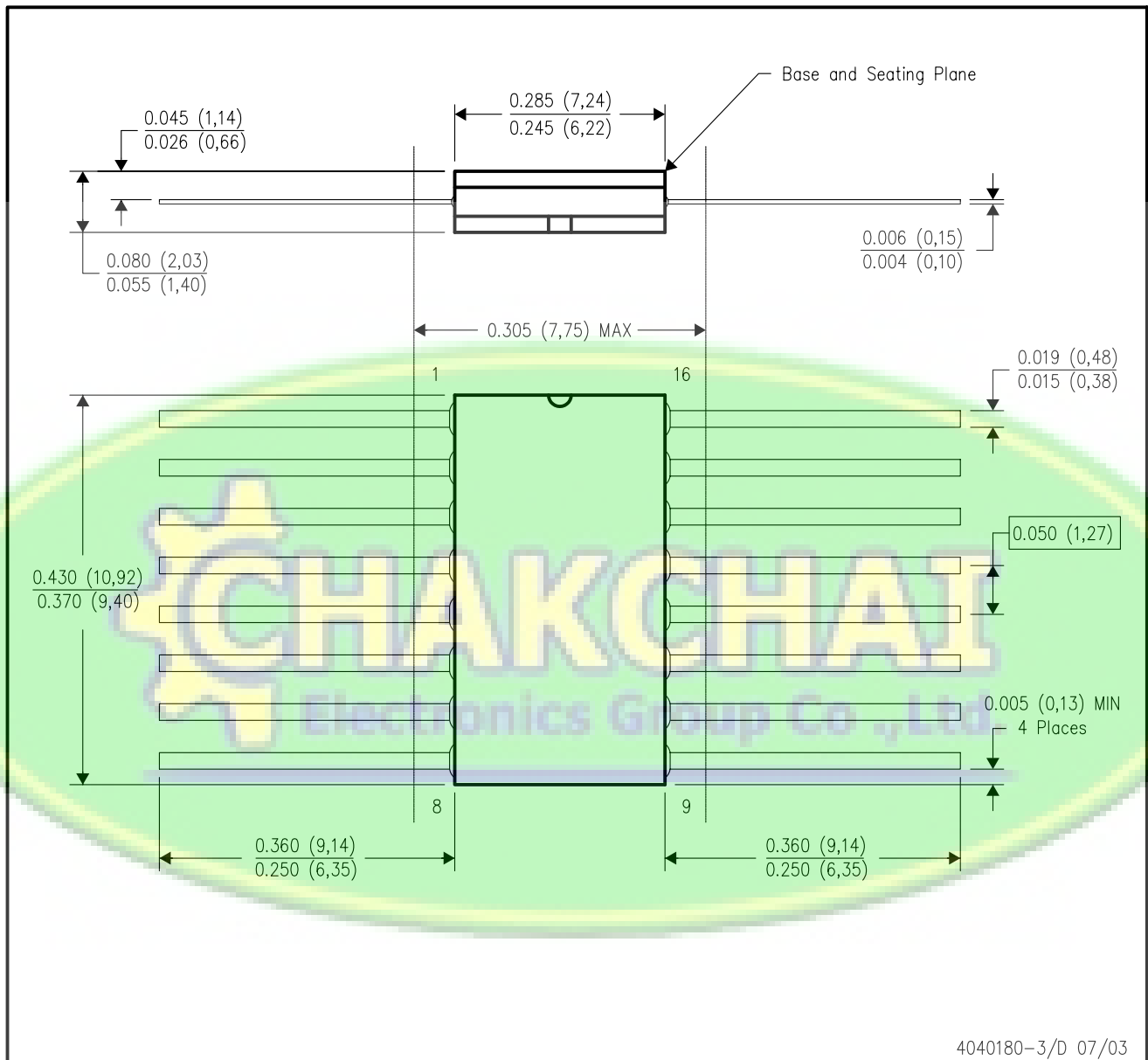0.100 (2,54)

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R−GDFP−F16)   CERAMIC DUAL FLATPACK

Base and Seating Plane

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.285\ (7,24)}{0.245\ (6,22)}$

$\dfrac{0.080\ (2,03)}{0.055\ (1,40)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

0.305 (7,75) MAX

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

1   16

0.050 (1,27)

$\dfrac{0.430\ (10,92)}{0.370\ (9,40)}$

0.005 (0,13) MIN
4 Places

8   9

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

$\dfrac{0.360\ (9,14)}{0.250\ (6,35)}$

4040180−3/D 07/03
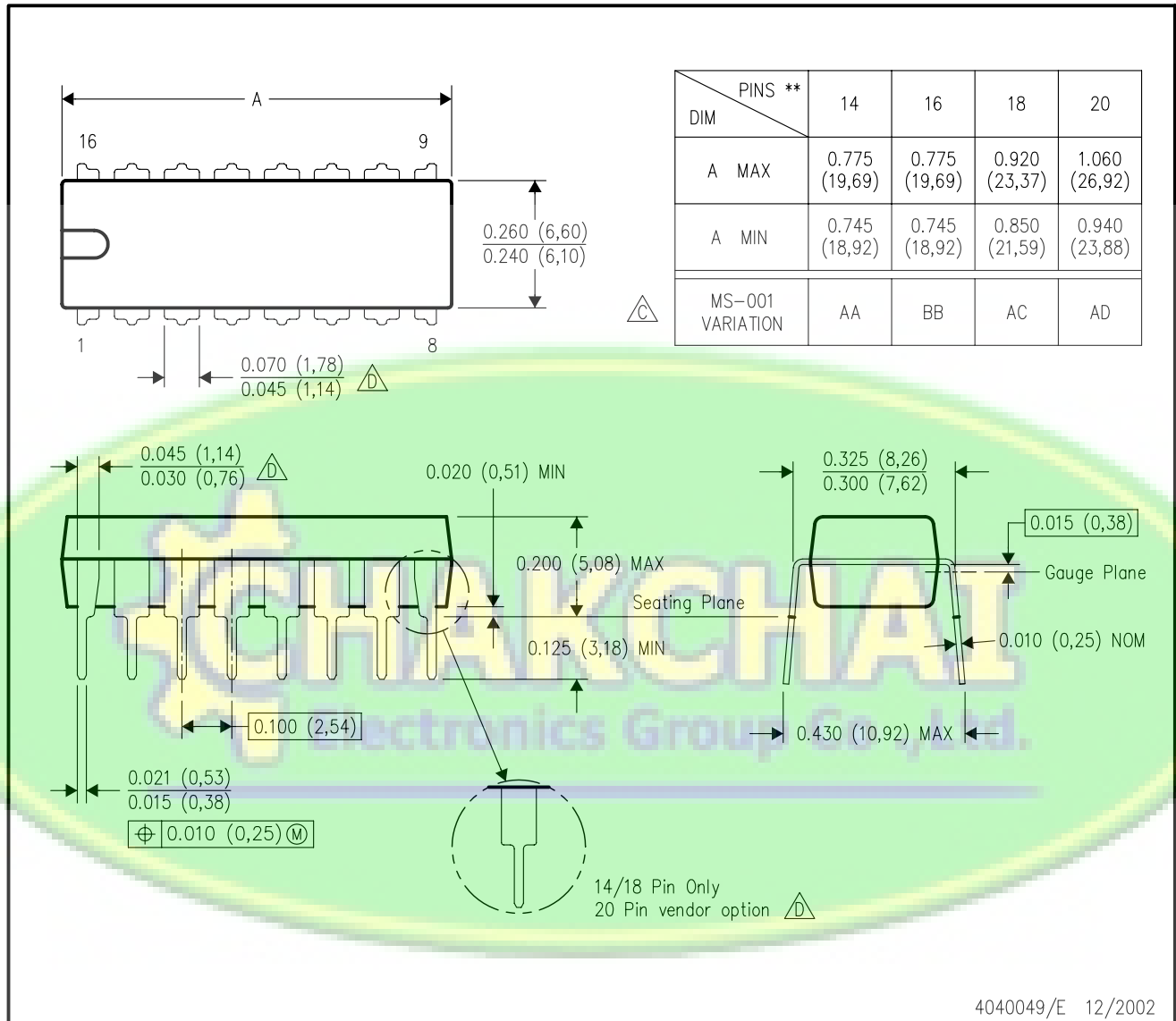
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
   E.   Falls within MIL STD 1835 GDFP1−F16 and JEDEC MO−092AC

TEXAS
INSTRUMENTS
www.ti.com

N (R-PDIP-T**)   PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)   △D

0.045 (1,14)
0.030 (0,76)   △D

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

Gauge Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

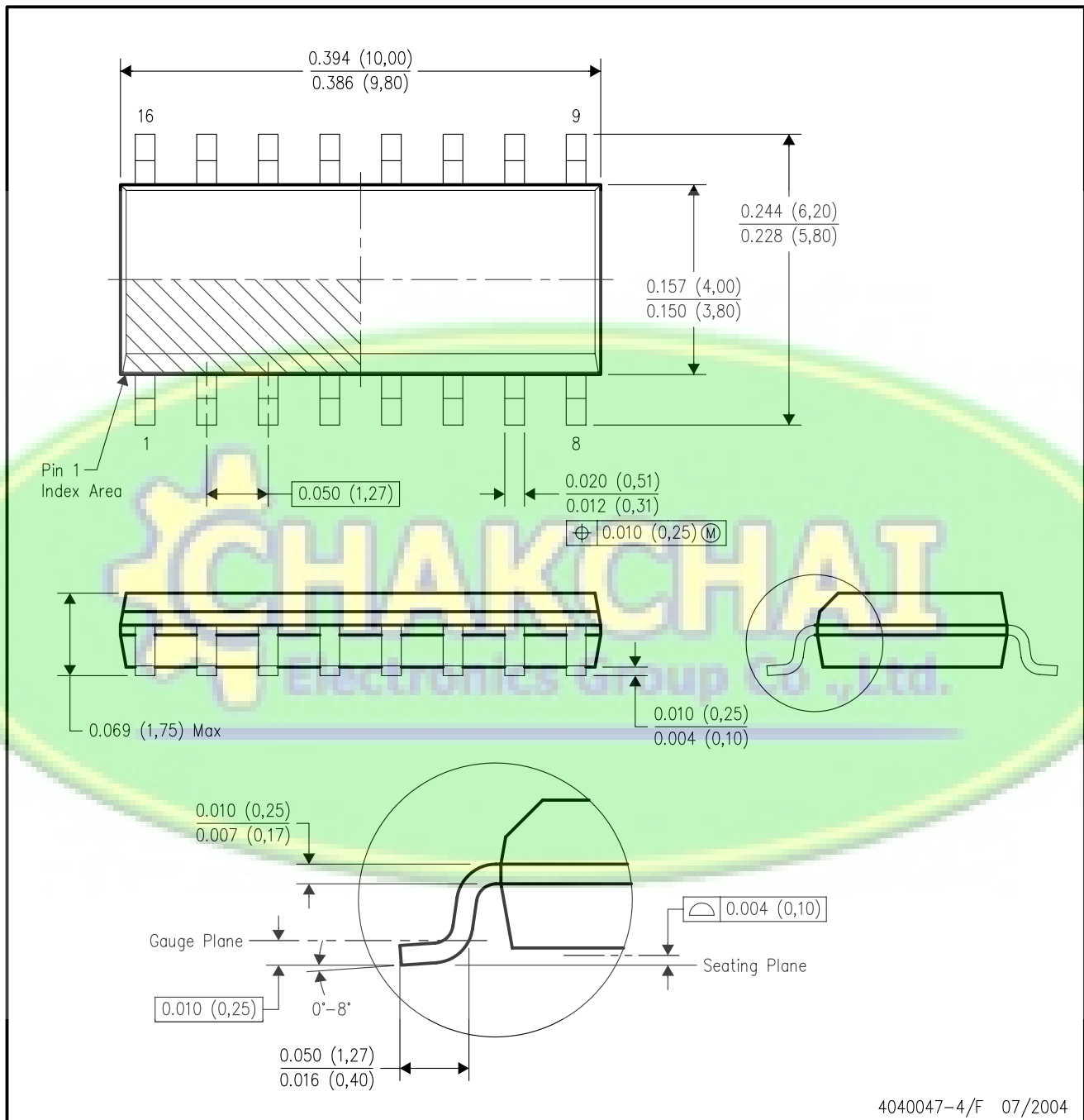14/18 Pin Only
20 Pin vendor option   △D

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      △C   Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
      △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.394 (10,00)
0.386 (9,80)

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

◁ | 0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−4/F   07/2004

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D. Falls within JEDEC MS−012 variation AC.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265