5472/7472 AND-Gated J-K Master-Slave Flip-Flop with Preset and Clear

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF
T.I.						SN54H72	J①			W②						SN5472	J①			W②	SN74L72	J①	N①	T②	
						SN74H72	J①	N①								SN7472	J①	N①			SN54L72	J①	N①	T②	
FAIRCHILD						FM54H72/FM9H72	D①			F②						FM5472/FM9N72	D①			F②					
						FC74H72/FC9H72	D①	P①		F②						FC7472/FC9N72	D①	P①		F②					
MOTOROLA						MC3155	L①			F①						MC5472	L①			F②					
						MC3055	L①	P①		F①						MC7472	L①	①		F②					
N.S.C.						DM54H72	J①	N①								DM5472	J①	N①		W②	DM54L72	J①	N①		F②
						DM74H72	J①	N①								DM7472	J①	N①			DM74L72	J①	N①		F②
PHILIPS																									
						GJJ111/74H72		①								FJJ111/7472		①							
SIGNETICS						S54H72	F①	A①		W②						S5472	F①	A①		W②					
						N74H72	F①	A①								N7472	F①	A①							
SIEMENS																									
																FLJ111		①							
FUJITSU						MB609	①	M①								MB407	①	M①							
HITACHI																									
																HD7472/HD2529	①	P①							
MITSUBISHI																									
																M53272/M5372		P①							
NEC																									
																μPB212	D①	C①							
TOSHIBA																									
																TD3472A		P①							

Electrical Characteristics SN5472/SN7472

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54'	−55°C to 125°C
Input voltage	5.5V		SN74'	0°C to 70°C
		Storage temperature range		−65°C to 150°C

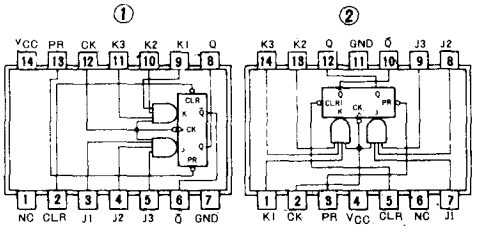
recommended operating conditions

		SN5472 MIN	NOM	MAX	SN7472 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				16			16	mA
Pulse width, t_w	Clock high	20			20			ns
	Clock low	47			47			
	Preset or clear low	25			25			
Input setup time, t_{setup}		0↑			0↑			ns
Input hold time, t_{hold}		5↓			5↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical chararacteristics over recommended operating free-air temperature range

PARAMETER *			TEST CONDITIONS †	MIN	TYP ‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC}=MIN, I_I=−12mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OH}=MAX	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=MIN, V_{IH}=2V, V_{IL}=0.8V, I_{OL}=16mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=5.5V			1	mA
I_{IH}	High-level input current	D, J, K, or K̄	V_{CC}=MAX, V_I=2.4V			40	μA
		Clear				80	
		Preset				80	
		Clock				80	
I_{IL}	Low-level input current	D, J, K, or K̄	V_{CC}=MAX, V_I=0.4V			−1.6	mA
		Clear				−3.2	
		Preset				−3.2	
		Clock				−3.2	
I_{OS}	Short-circuit output current ◆	Series 54	V_{CC}=MAX	−20		−57	mA
		Series 74		−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC}=MAX, See Note 1		10	20	mA
f_{max}	maximum clock frequency		V_{CC}=5V, T_A=25°C, C_L=15pF, R_L=400Ω	15	20		MHz
t_{PLH}	from Preset to output Q (as applicable)				16	25	ns
t_{PHL}	from Preset to output Q̄ (as paplicable)				25	40	
t_{PLH}	from Clear to output Q̄ (as applicable)				16	25	ns
t_{PHL}	from Clear to output Q (as applicable)				25	40	
t_{PLH}	from Clock to output Q or Q̄				16	25	ns
t_{PHL}					25	40	

Pin Assignments (Top View)



NC—No internal connection

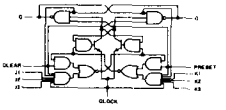
Function Table

'72, 'H72, 'L71 (See Note 2)

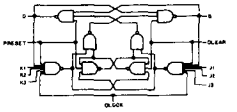
INPUTS PRESET	CLEAR	CLOCK	J	K	OUTPUTS Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	

positive logic: $\overline{1}=\overline{J1}\cdot\overline{J2}\cdot\overline{J3}; \overline{K1}\cdot\overline{K2}\cdot\overline{K3}$

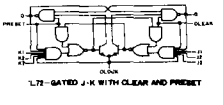
Functional Block Diagrams



'72—GATED J-K WITH CLEAR AND PRESET



'H72—GATED J-K WITH CLEAR AND PRESET



'L72—GATED J-K WITH CLEAR AND PRESET

NOTES: 1. With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

2. H=high level (steady state), L=low level (state), X=irrelevant
   ⎍=high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
   Q_0=the level of Q before the indicated input conditions were established.
   TOGGLE: Each output changes to the complemplement of its previous level on each active transition (pulse) of the clock.
   • This configuration is nonstable; that is, it presist when preset and clear inputs return to their inactive (high) level.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC}=5V, T_A=25°C.
◆*Not more than one output should be shorted at a time.*
*t_{PLH}=propagation delay time, low-to-high-level output; t_{PHL}=propagation delay time, high-to-low-level output.
↓↑The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.