

110MHz, High Slew Rate, High Output Current Buffer

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Intersil D.I. technologies, the HA-5002 current buffer offers 1300V/ μ s slew rate with 110MHz of bandwidth. The ± 200 mA output current capability is enhanced by a 3 Ω output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000k Ω input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

For the military grade product, refer to the HA-5002/883 datasheet, AnswerFAX document #3705.

Features

- Voltage Gain 0.995
- High Input Impedance 3000k Ω
- Low Output Impedance 3 Ω
- Very High Slew Rate 1300V/ μ s
- Very Wide Bandwidth 110MHz
- High Output Current ± 200 mA
- Pulsed Output Current 400mA
- Monolithic Construction

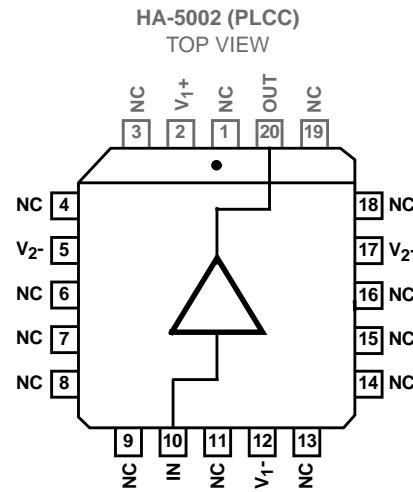
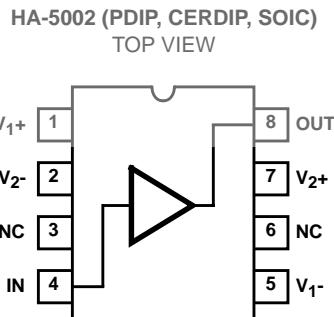
Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- Radar Cable Driver
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Video Products

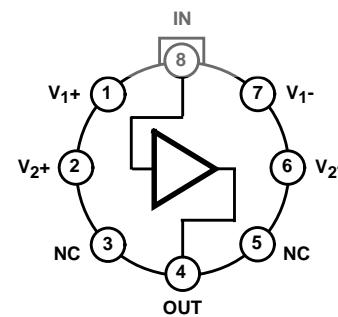
Ordering Information

| PART NUMBER (BRAND) | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|------------------------|---------------------|-----------------|----------|
| HA2-5002-2 | -55 to 125 | 8 Pin Metal Can | T8.C |
| HA2-5002-5 | 0 to 75 | 8 Pin Metal Can | T8.C |
| HA3-5002-5 | 0 to 75 | 8 Ld PDIP | E8.3 |
| HA4P5002-5 | 0 to 75 | 20 Ld PLCC | N20.35 |
| HA7-5002-2 | -55 to 125 | 8 Ld CERDIP | F8.3A |
| HA7-5002-5 | 0 to 75 | 8 Ld CERDIP | F8.3A |
| HA9P5002-5 (H50025) | 0 to 75 | 8 Ld SOIC | M8.15 |
| HA9P5002-9 (H50029) | -40 to 85 | 8 Ld SOIC | M8.15 |

Pinouts



HA-5002 (METAL CAN)
TOP VIEW



NOTE: Case Voltage = Floating

Absolute Maximum Ratings

| | |
|--|------------------------------------|
| Voltage Between V+ and V- Terminals..... | 44V |
| Input Voltage | V ₁₊ to V ₁₋ |
| Output Current (Continuous) | ±200mA |
| Output Current (50ms On, 1s Off) | ±400mA |

Operating Conditions

| | |
|-------------------|----------------|
| Temperature Range | |
| HA-5002-2 | -55°C to 125°C |
| HA-5002-5 | 0°C to 75°C |
| HA-5002-9 | -40°C to 85°C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below 175°C for the ceramic and can packages, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | HA-5002-2 | | | HA-5002-5, -9 | | | UNITS |
|--|--|-----------|-----------|--------|-----|---------------|--------|-----|-------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| INPUT CHARACTERISTICS | | | | | | | | | |
| Offset Voltage | | 25 | - | 5 | 20 | - | 5 | 20 | mV |
| | Full | - | 10 | 30 | - | 10 | 30 | - | mV |
| Average Offset Voltage Drift | Full | - | 30 | - | - | 30 | - | - | µV/°C |
| Bias Current | 25 | - | 2 | 7 | - | 2 | 7 | - | µA |
| | Full | - | 3.4 | 10 | - | 2.4 | 10 | - | µA |
| Input Resistance | | Full | 1.5 | 3 | - | 1.5 | 3 | - | MΩ |
| Input Noise Voltage | 10Hz-1MHz | 25 | - | 18 | - | - | 18 | - | µV _{P-P} |
| TRANSFER CHARACTERISTICS | | | | | | | | | |
| Voltage Gain (V _{OUT} = ±10V) | R _L = 50Ω | 25 | - | 0.900 | - | - | 0.900 | - | V/V |
| | R _L = 100Ω | 25 | - | 0.971 | - | - | 0.971 | - | V/V |
| | R _L = 1kΩ | 25 | - | 0.995 | - | - | 0.995 | - | V/V |
| | R _L = 1kΩ | Full | 0.980 | - | - | 0.980 | - | - | V/V |
| -3dB Bandwidth | V _{IN} = 1V _{P-P} | 25 | - | 110 | - | - | 110 | - | MHz |
| AC Current Gain | | 25 | - | 40 | - | - | 40 | - | A/mA |
| OUTPUT CHARACTERISTICS | | | | | | | | | |
| Output Voltage Swing | R _L = 100Ω | 25 | ±10 | ±10.7 | - | ±10 | ±11.2 | - | V |
| | R _L = 1kΩ, V _S = ±15V | Full | ±10 | ±13.5 | - | ±10 | ±13.9 | - | V |
| | R _L = 1kΩ, V _S = ±12V | Full | ±10 | ±10.5 | - | ±10 | ±10.5 | - | V |
| Output Current | V _{IN} = ±10V, R _L = 40Ω | 25 | - | 220 | - | - | 220 | - | mA |
| Output Resistance | | Full | - | 3 | 10 | - | 3 | 10 | Ω |
| Harmonic Distortion | V _{IN} = 1VRMS, f = 10kHz | 25 | - | <0.005 | - | - | <0.005 | - | % |
| TRANSIENT RESPONSE | | | | | | | | | |
| Full Power Bandwidth (Note 3) | | 25 | - | 20.7 | - | - | 20.7 | - | MHz |
| Rise Time | | 25 | - | 3.6 | - | - | 3.6 | - | ns |
| Propagation Delay | | 25 | - | 2 | - | - | 2 | - | ns |
| Overshoot | | 25 | - | 30 | - | - | 30 | - | % |
| Slew Rate | | 25 | 1.0 | 1.3 | - | 1.0 | 1.3 | - | V/ns |
| Settling Time | To 0.1% | 25 | - | 50 | - | - | 50 | - | ns |
| Differential Gain | R _L = 500Ω | 25 | - | 0.06 | - | - | 0.06 | - | % |
| Differential Phase | R _L = 500Ω | 25 | - | 0.22 | - | - | 0.22 | - | Degrees |

Thermal Information

| | | |
|---|----------------------|----------------------|
| Thermal Resistance (Typical, Note 2) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| CERDIP Package..... | 115 | 28 |
| PDIP Package | 92 | N/A |
| Metal Can Package | 155 | 67 |
| PLCC Package..... | 74 | N/A |
| SOIC Package | 157 | N/A |
| Max Junction Temperature (Hermetic Packages, Note 1) | 175°C | |
| Max Junction Temperature (Plastic Packages, Note 1) | 150°C | |
| Max Storage Temperature Range | -65°C to 150°C | |
| Max Lead Temperature (Soldering 10s) (PLCC and SOIC - Lead Tips Only) | 300°C | |

Electrical Specifications V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | HA-5002-2 | | | HA-5002-5, -9 | | | UNITS |
|------------------------------|----------------------|-----------|-----------|-----|-----|---------------|-----|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| POWER REQUIREMENTS | | | | | | | | | |
| Supply Current | | 25 | - | 8.3 | - | - | 8.3 | - | mA |
| | | Full | - | - | 10 | - | - | 10 | mA |
| Power Supply Rejection Ratio | A _V = 10V | Full | 54 | 64 | - | 54 | 64 | - | dB |

NOTE:

3. PBW = $\frac{\text{Slew Rate}}{2\pi V_{\text{PEAK}}} ; V_P = 10V \cdot$

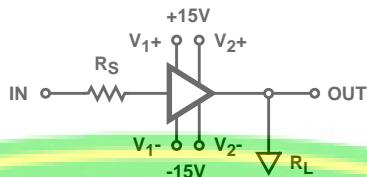
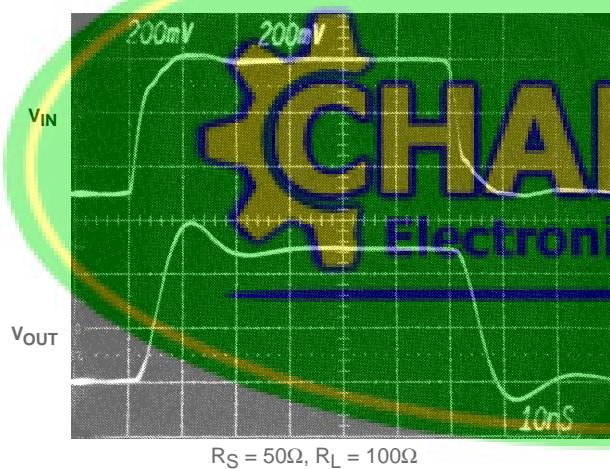
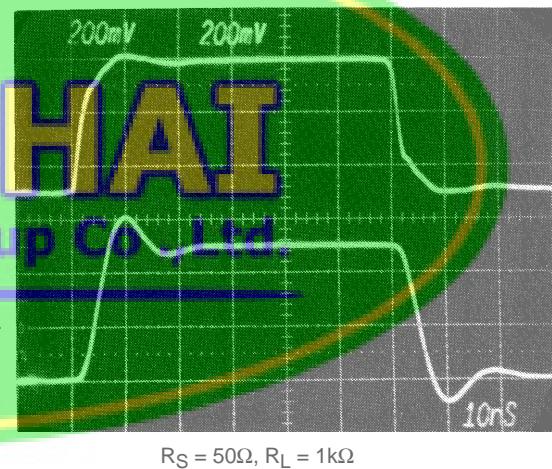
Test Circuit and Waveforms

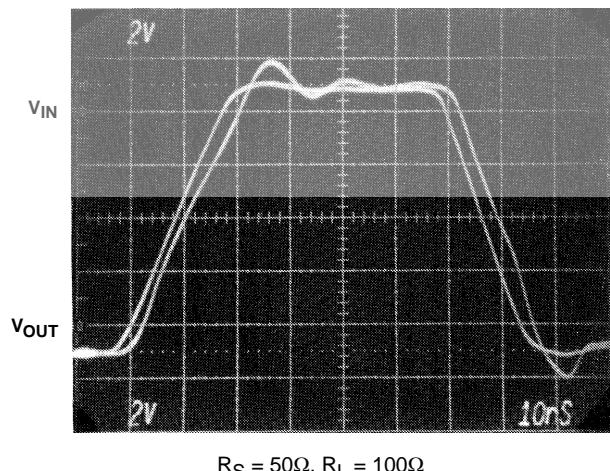
FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE



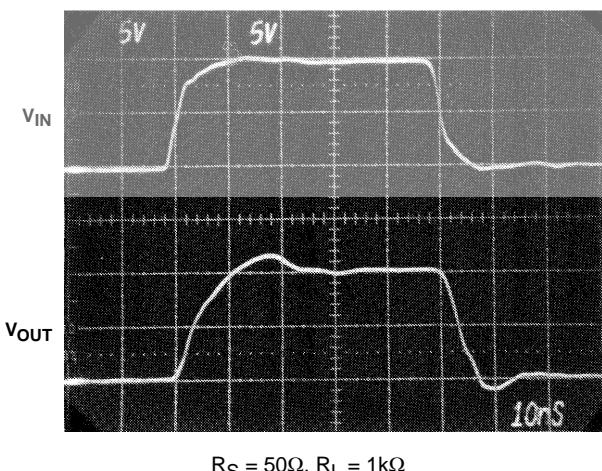
SMALL SIGNAL WAVEFORMS



SMALL SIGNAL WAVEFORMS

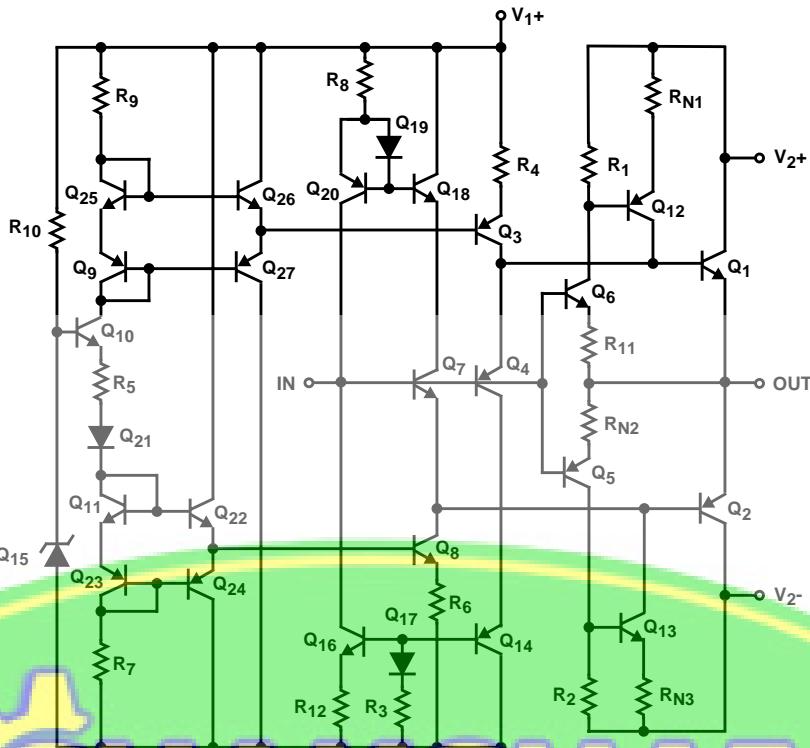


LARGE SIGNAL WAVEFORMS



LARGE SIGNAL WAVEFORMS

Schematic Diagram



Application Information

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to $0.1\mu\text{F}$ will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

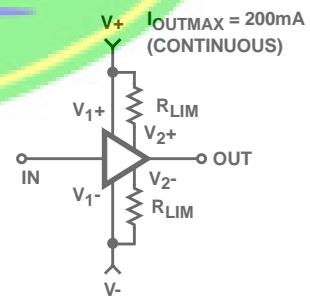
Operation at Reduced Supply Levels

The HA-5002 can operate at supply voltage levels as low as $\pm 5\text{V}$ and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

Short Circuit Protection

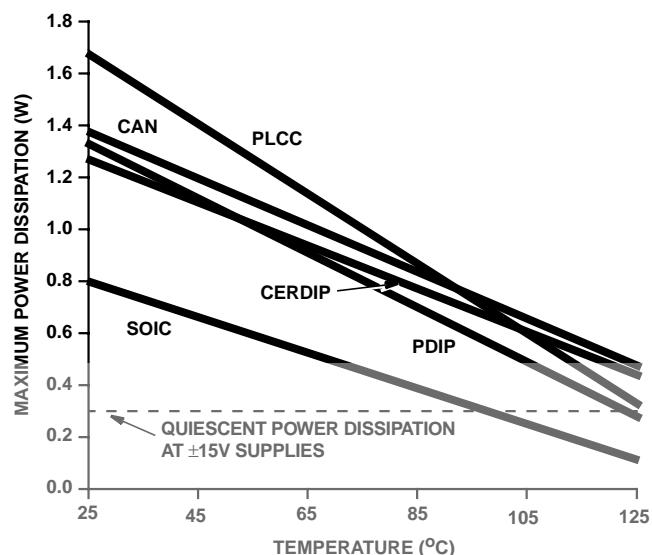
The output current can be limited by using the following circuit:

$$R_{\text{LIM}} = \frac{V_+ - V_-}{I_{\text{OUTMAX}}} = \frac{V_-}{I_{\text{OUTMAX}}}$$



Capacitive Loading

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula $I = Cdv/dt$ implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to $1\text{k}\Omega$; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10Ω to 50Ω ; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.



$$P_{D\text{MAX}} = \frac{T_{J\text{MAX}} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where: $T_{J\text{MAX}}$ = Maximum Junction Temperature of the Device
 T_A = Ambient

θ_{JC} = Junction to Case Thermal Resistance

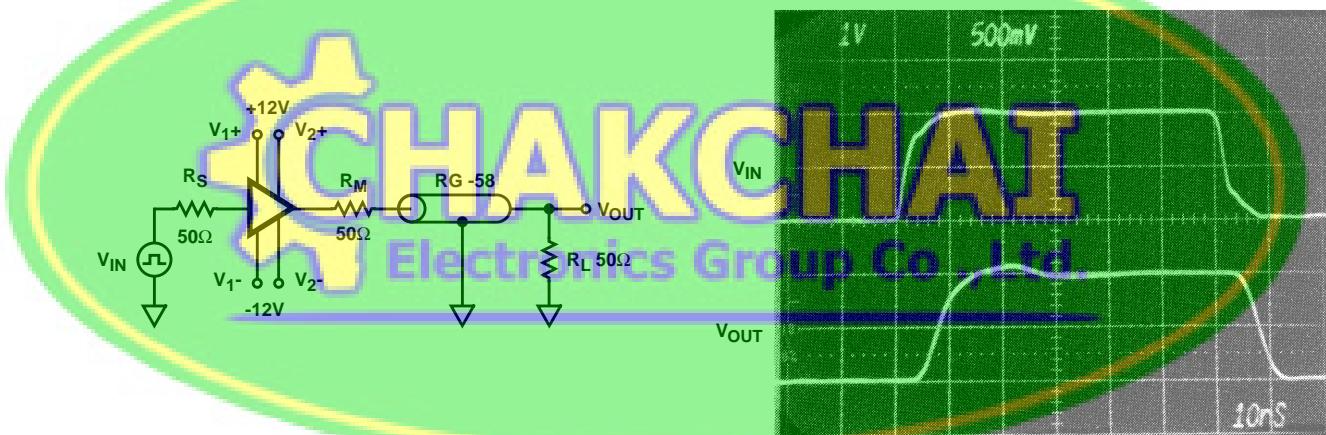
θ_{CS} = Case to Heat Sink Thermal Resistance

θ_{SA} = Heat Sink to Ambient Thermal Resistance

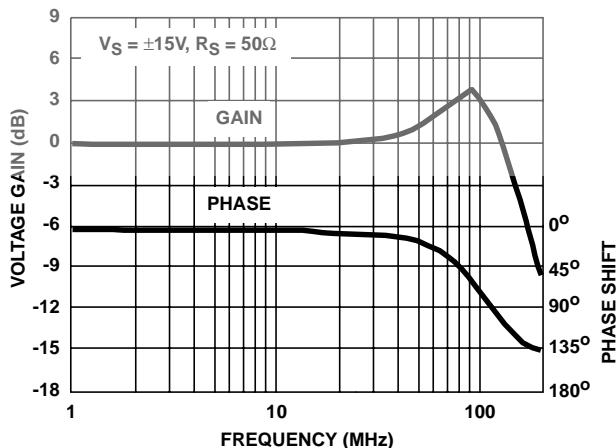
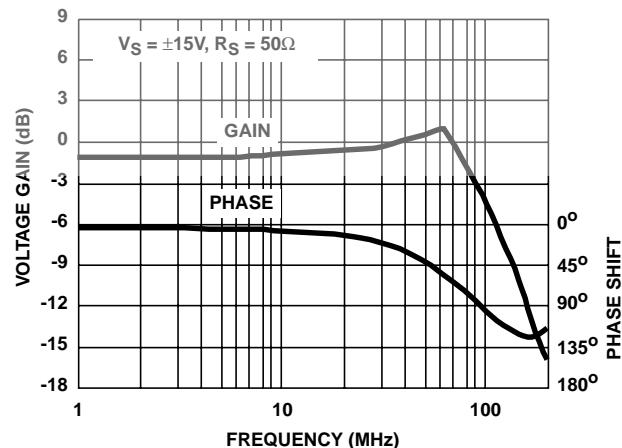
$$\text{Graph is based on: } P_{D\text{MAX}} = \frac{T_{J\text{MAX}} - T_A}{\theta_{JA}}$$

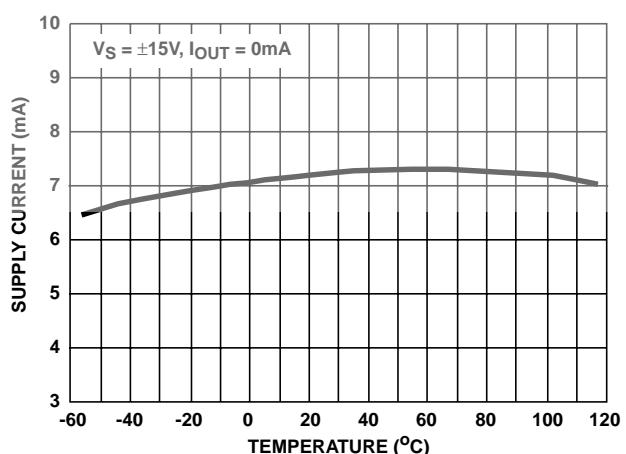
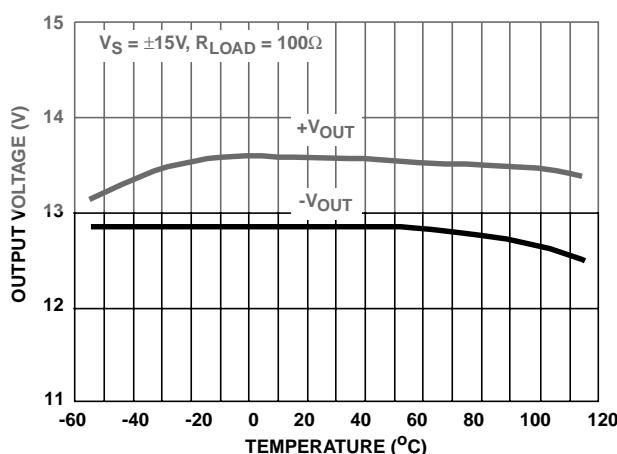
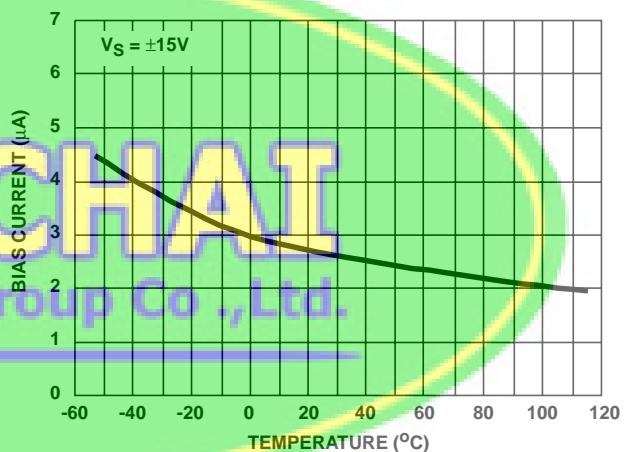
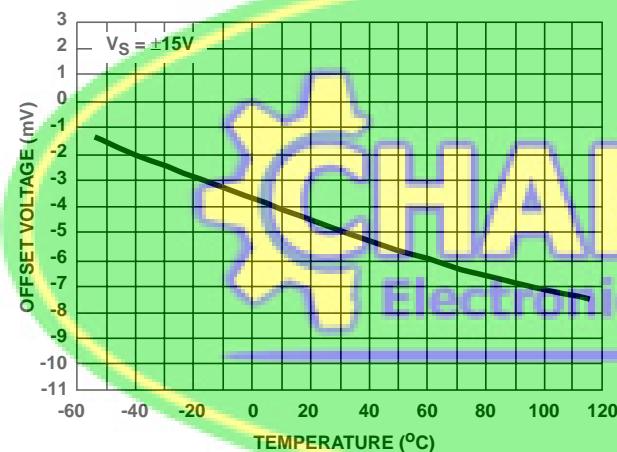
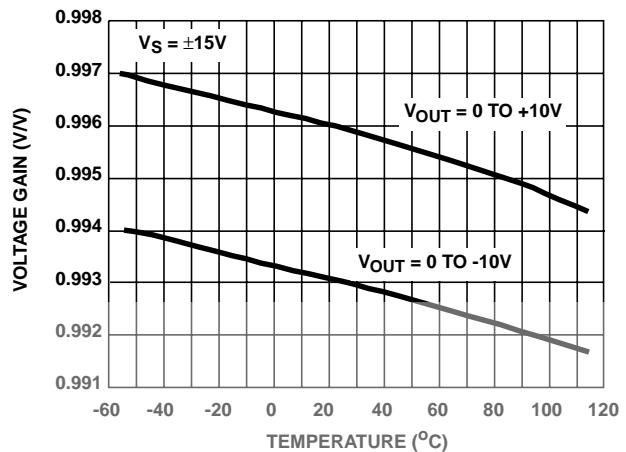
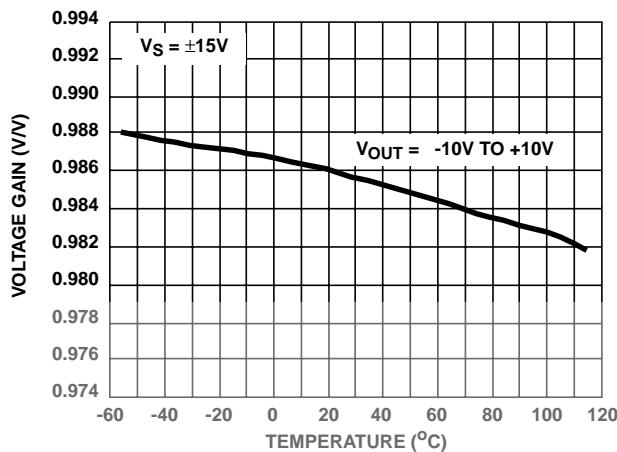
FIGURE 2. MAXIMUM POWER DISSIPATION vs TEMPERATURE

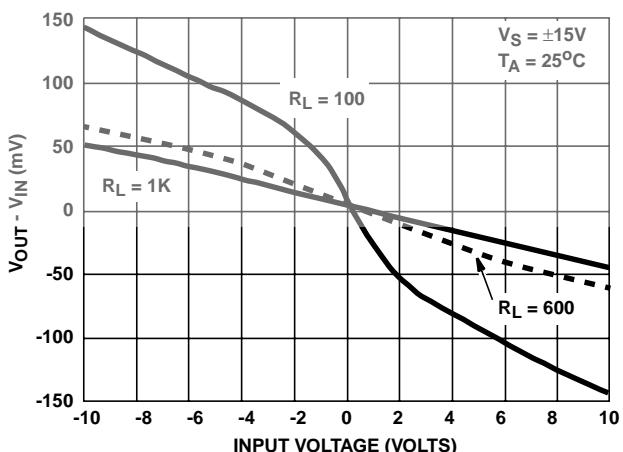
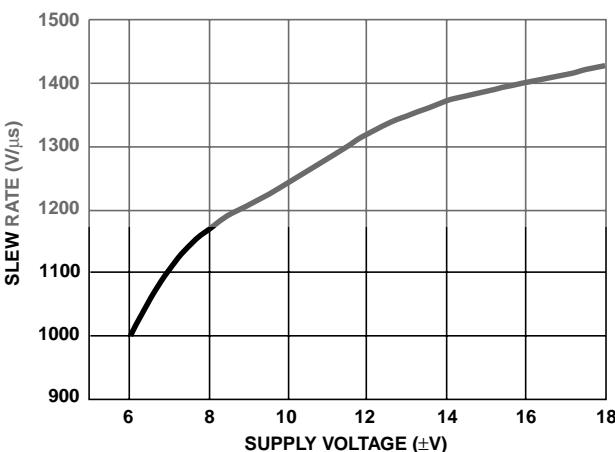
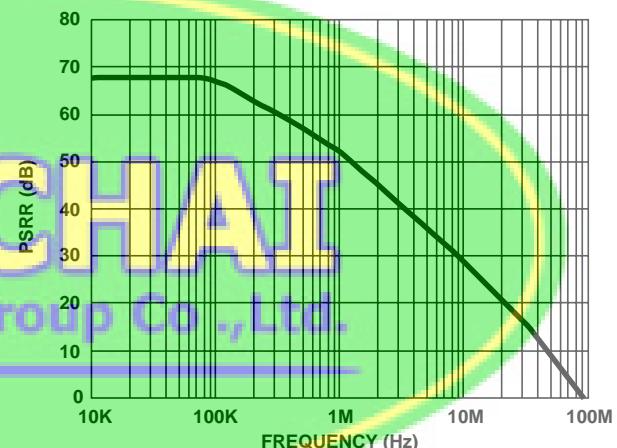
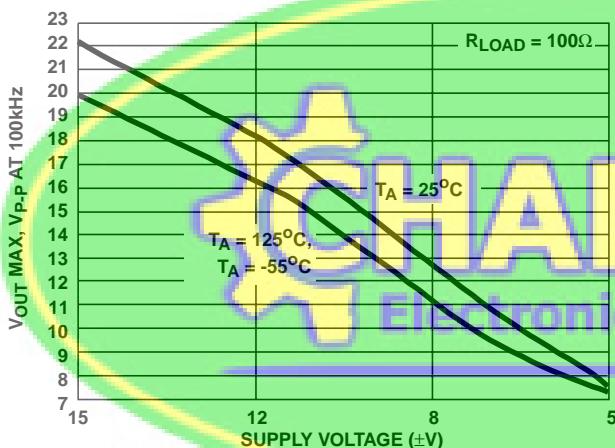
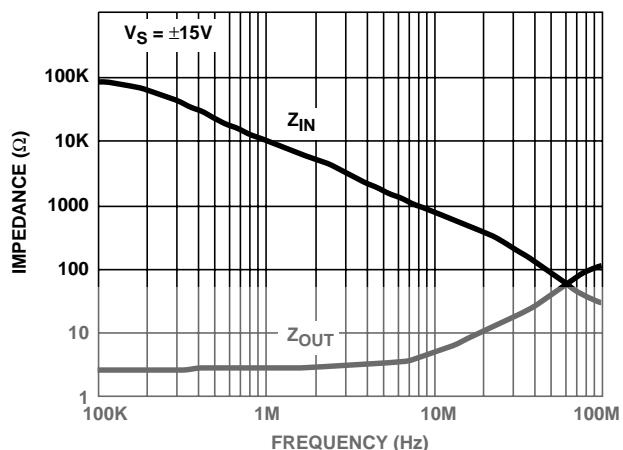
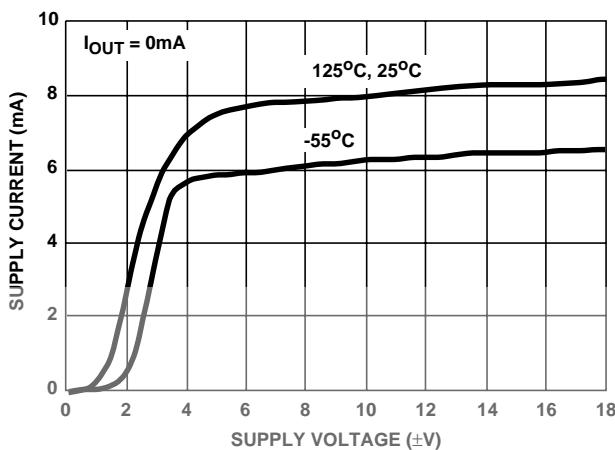
Typical Application

FIGURE 3. COAXIAL CABLE DRIVER - 50Ω SYSTEM

Typical Performance Curves

FIGURE 4. GAIN/PHASE vs FREQUENCY ($R_L = 1k\Omega$)FIGURE 5. GAIN/PHASE vs FREQUENCY ($R_L = 50\Omega$)

Typical Performance Curves (Continued)

Typical Performance Curves (Continued)

Die Characteristics**DIE DIMENSIONS:**

81 mils x 80 mils x 19 mils
2050 μ m x 2030 μ m x 483 μ m

METALLIZATION:

Type: Al, 1% Cu
Thickness: 20k \AA \pm 2k \AA

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2 , 5% Phos.)
Silox Thickness: 12k \AA \pm 2k \AA
Nitride Thickness: 3.5k \AA \pm 1.5k \AA

SUBSTRATE POTENTIAL (Powered Up):

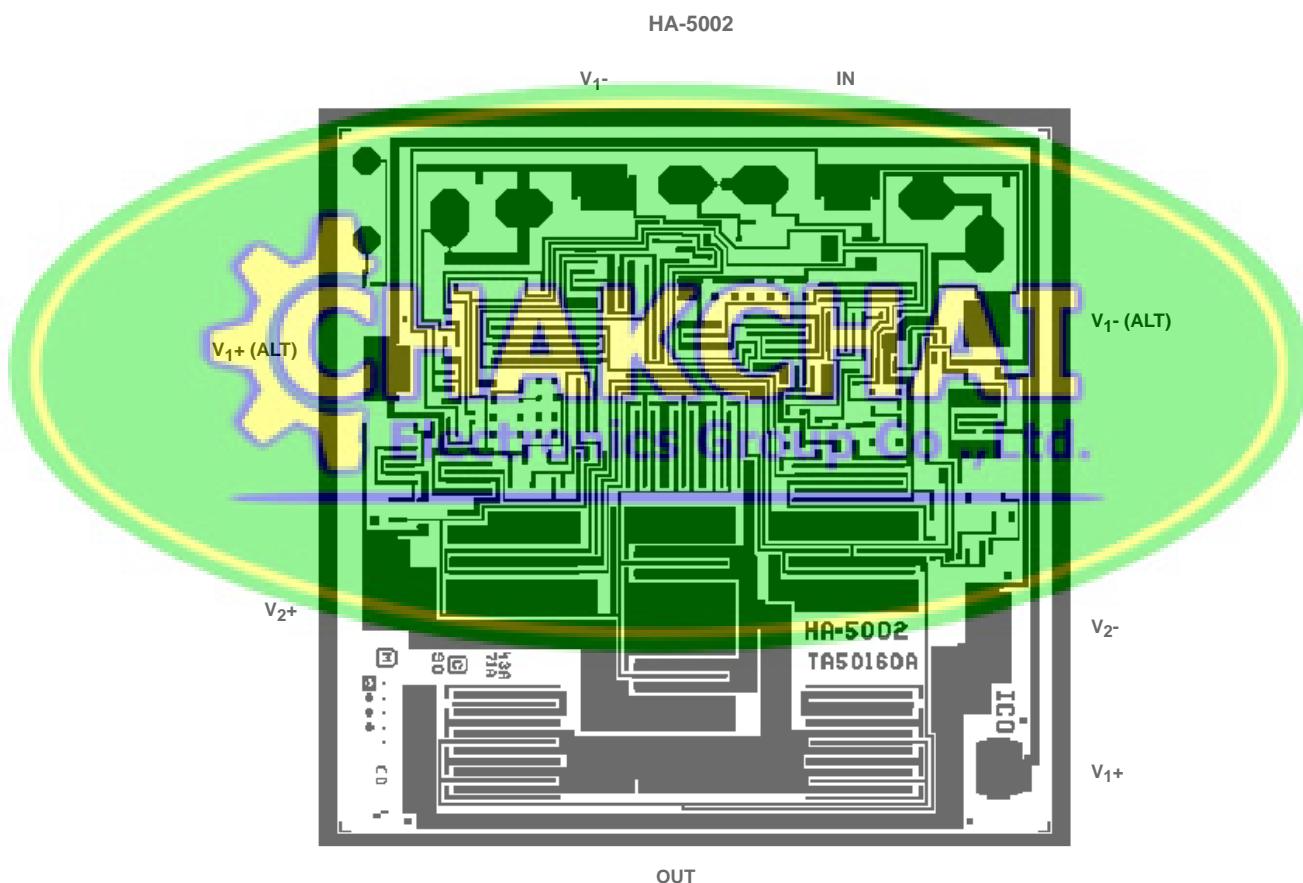
V₁₋

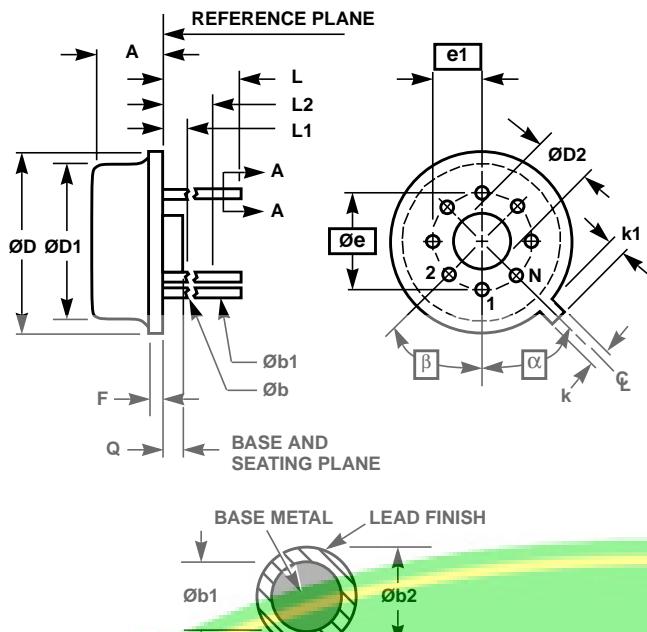
TRANSISTOR COUNT:

27

PROCESS:

Bipolar Dielectric Isolation

Metalization Mask Layout

Metal Can Packages (Can)

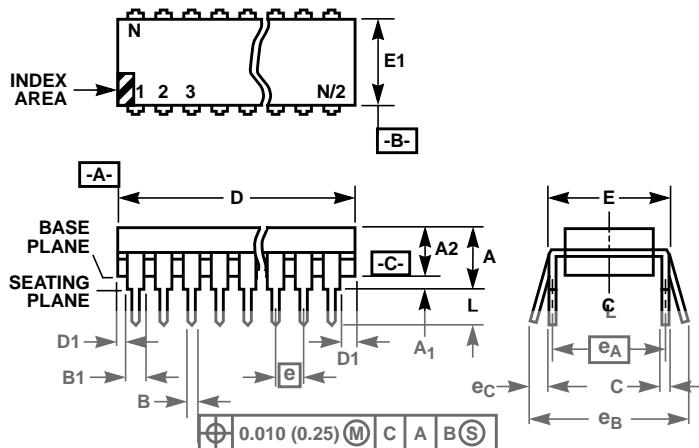
NOTES:

- (All leads) $\varnothing b$ applies between L1 and L2. $\varnothing b_1$ applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
- Measured from maximum diameter of the product.
- α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α , looking at the bottom of the package.
- N is the maximum number of terminal positions.
- Dimensioning and tolerancing per ANSI Y14.5M - 1982.
- Controlling dimension: INCH.

**T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|-------------------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.165 | 0.185 | 4.19 | 4.70 | - |
| $\varnothing b$ | 0.016 | 0.019 | 0.41 | 0.48 | 1 |
| $\varnothing b_1$ | 0.016 | 0.021 | 0.41 | 0.53 | 1 |
| $\varnothing b_2$ | 0.016 | 0.024 | 0.41 | 0.61 | - |
| $\varnothing D$ | 0.335 | 0.375 | 8.51 | 9.40 | - |
| $\varnothing D_1$ | 0.305 | 0.335 | 7.75 | 8.51 | - |
| $\varnothing D_2$ | 0.110 | 0.160 | 2.79 | 4.06 | - |
| e | 0.200 BSC | | 5.08 BSC | | - |
| e1 | 0.100 BSC | | 2.54 BSC | | - |
| F | - | 0.040 | - | 1.02 | - |
| k | 0.027 | 0.034 | 0.69 | 0.86 | - |
| k1 | 0.027 | 0.045 | 0.69 | 1.14 | 2 |
| L | 0.500 | 0.750 | 12.70 | 19.05 | 1 |
| L1 | - | 0.050 | - | 1.27 | 1 |
| L2 | 0.250 | - | 6.35 | - | 1 |
| Q | 0.010 | 0.045 | 0.25 | 1.14 | - |
| α | 45° BSC | | 45° BSC | | 3 |
| β | 45° BSC | | 45° BSC | | 3 |
| N | 8 | | 8 | | 4 |

Rev. 0 5/18/94

Dual-In-Line Plastic Packages (PDIP)

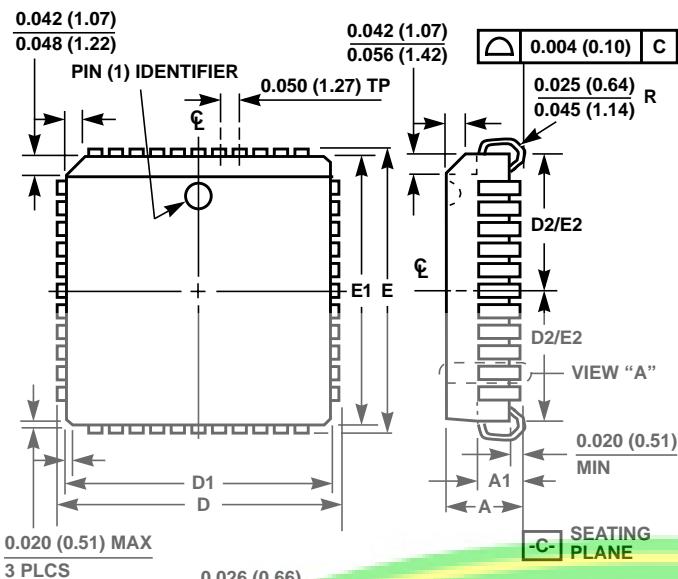
NOTES:

7. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
10. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
11. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
12. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
13. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
14. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
15. N is the maximum number of terminal positions.
16. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.355 | 0.400 | 9.01 | 10.16 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| e_A | 0.300 BSC | | 7.62 BSC | | 6 |
| e_B | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 8 | | 8 | | 9 |

Rev. 0 12/93

Plastic Leaded Chip Carrier Packages (PLCC)

N20.35 (JEDEC MS-018AA ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

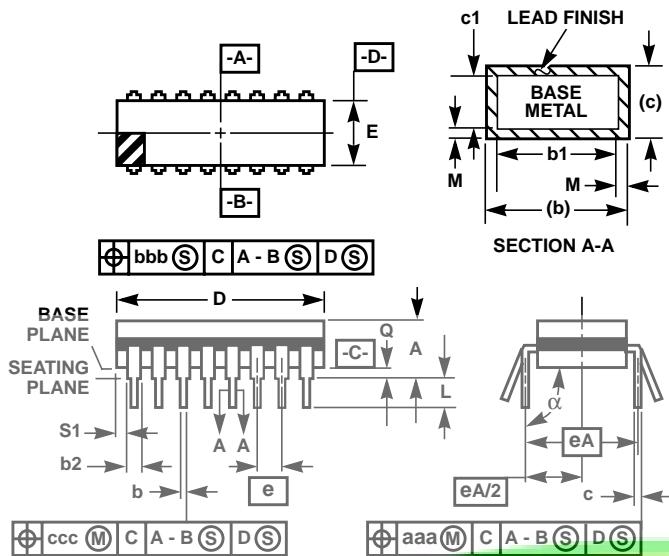
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.165 | 0.180 | 4.20 | 4.57 | - |
| A1 | 0.090 | 0.120 | 2.29 | 3.04 | - |
| D | 0.385 | 0.395 | 9.78 | 10.03 | - |
| D1 | 0.350 | 0.356 | 8.89 | 9.04 | 3 |
| D2 | 0.141 | 0.169 | 3.59 | 4.29 | 4, 5 |
| E | 0.385 | 0.395 | 9.78 | 10.03 | - |
| E1 | 0.350 | 0.356 | 8.89 | 9.04 | 3 |
| E2 | 0.141 | 0.169 | 3.59 | 4.29 | 4, 5 |
| N | 20 | | 20 | | 6 |

Rev. 2 11/97

NOTES:

17. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
18. Dimensions and tolerancing per ANSI Y14.5M-1982.
19. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
20. To be measured at seating plane **-C-** contact point.
21. Centerline to be determined where center leads exit plastic body.
22. "N" is the number of terminal positions.

CHAKCHAI
Electronics Group Co.,Ltd.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)

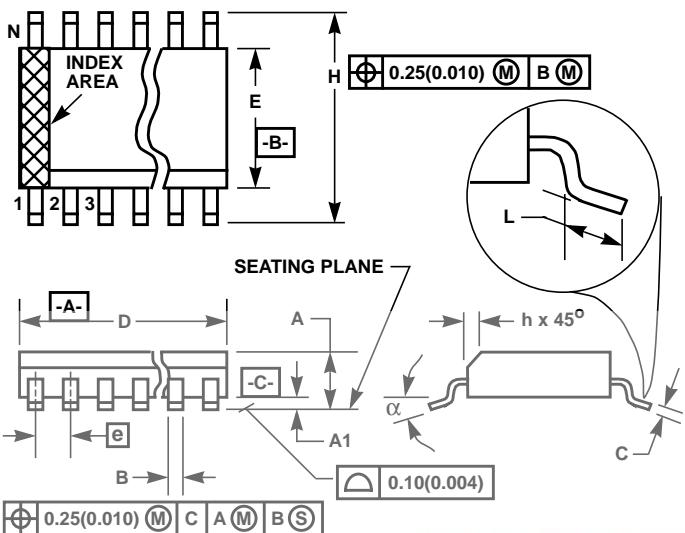
NOTES:

23. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
24. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
25. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
26. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
27. This dimension allows for off-center lid, meniscus, and glass overrun.
28. Dimension Q shall be measured from the seating plane to the base plane.
29. Measure dimension S1 at all four corners.
30. N is the maximum number of terminal positions.
31. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
32. Controlling dimension: INCH

**F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.405 | - | 10.29 | 5 |
| E | 0.220 | 0.310 | 5.59 | 7.87 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 6 |
| S1 | 0.005 | - | 0.13 | - | 7 |
| α | 90° | 105° | 90° | 105° | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2,3 |
| N | 8 | | 8 | | 8 |

Rev. 0 4/94

Small Outline Plastic Packages (SOIC)

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|--------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 0 12/93

NOTES:

33. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
34. Dimensioning and tolerancing per ANSI Y14.5M-1982.
35. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
36. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
37. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
38. "L" is the length of terminal for soldering to a substrate.
39. "N" is the number of terminal positions.
40. Terminal numbers are shown for reference only.
41. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
42. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com

Sales Office Headquarters**NORTH AMERICA**

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusée
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029