

DATA SHEET



80C51/87C51/80C31

80C51 8-bit microcontroller family
4K/128 OTP/ROM/ROMless low voltage (2.7V–5.5V),
low power, high speed (33 MHz)

Product specification
Supersedes data of 1999 Apr 01
IC28 Data Handbook

2000 Jan 20

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DESCRIPTION

The Philips 8XC51/31 is a high-performance static 80C51 design fabricated with Philips high-density CMOS technology with operation from 2.7V to 5.5V.

The 8XC51/31 contains a 4k × 8 ROM, a 128 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device is a low power static design which offers a wide range of operating frequencies down to zero. Two software selectable modes of power reduction—idle mode and power-down mode are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data and then the execution resumed from the point the clock was stopped.

SELECTION TABLE

For applications requiring more ROM and RAM, see the 8XC52/54/58/80C32, 8XC51FA/FB/FC/80C51FA, and 8XC51RA+/RB+/RC+/80C51RA+ data sheet.

ROM/EPROM Memory Size (X by 8)	RAM Size (X by 8)	Programmable Timer Counter (PCA)	Hardware Watch Dog Timer
80C31/8XC51			
0K/4K	128	No	No
80C32/8XC52/54/58			
0K/8K/16K/32K	256	No	No
80C51FA/8XC51FA/FB/FC			
0K/8K/16K/32K	256	Yes	No
80C51RA+/8XC51RA+/RB+/RC+			
0K/8K/16K/32K	512	Yes	Yes
8XC51RD+			
64K	1024	Yes	Yes

FEATURES

- 8051 Central Processing Unit
 - 4k × 8 ROM (80C51)
 - 128 × 8 RAM
 - Three 16-bit counter/timers
 - Boolean processor
 - Full static operation
 - Low voltage (2.7V to 5.5V@ 16MHz) operation
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Clock can be stopped and resumed
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- TWO speed ranges at $V_{CC} = 5V$
 - 0 to 16MHz
 - 0 to 33MHz
- Three package styles
- Extended temperature ranges
- Dual Data Pointers
- Security bits:
 - ROM (2 bits)
 - OTP/EPROM (3 bits)
- Encryption array—64 bytes
- 4 level priority interrupt
- 6 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Programmable clock out
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Wake-up from Power Down by an external interrupt (8XC51)

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80C51/87C51 AND 80C31 ORDERING INFORMATION

	MEMORY SIZE 4K × 8	ROMless	TEMPERATURE RANGE °C AND PACKAGE	VOLTAGE RANGE	FREQ. (MHz)	DWG. #
ROM	P80C51SBPN	P80C31SBPN	0 to +70, Plastic Dual In-line Package	2.7V to 5.5V	0 to 16	SOT129-1
OTP	P87C51SBPN					
ROM	P80C51SBAA	P80C31SBAA	0 to +70, Plastic Leaded Chip Carrier	2.7V to 5.5V	0 to 16	SOT187-2
OTP	P87C51SBAA					
ROM	P80C51SBBB	P80C31SBBB	0 to +70, Plastic Quad Flat Pack	2.7V to 5.5V	0 to 16	SOT307-2
OTP	P87C51SBBB					
ROM	P80C51SFPN	P80C31SFPN	-40 to +85, Plastic Dual In-line Package	2.7V to 5.5V	0 to 16	SOT129-1
OTP	P87C51SFPN					
ROM	P80C51SFA A	P80C31SFA A	-40 to +85, Plastic Leaded Chip Carrier	2.7V to 5.5V	0 to 16	SOT187-2
OTP	P87C51SFA A					
ROM	P80C51SFBB	P80C31SFBB	-40 to +85, Plastic Quad Flat Pack	2.7V to 5.5V	0 to 16	SOT307-2
OTP	P87C51SFBB					
ROM	P80C51UBAA	P80C31UBAA	0 to +70, Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
OTP	P87C51UBAA					
ROM	P80C51UBPN	P80C31UBPN	0 to +70, Plastic Dual In-line Package	5V	0 to 33	SOT129-1
OTP	P87C51UBPN					
ROM	P80C51UBBB	P80C31UBBB	0 to +70, Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
OTP	P87C51UBBB					
ROM	P80C51UFA A	P80C31UFA A	-40 to +85, Plastic Leaded Chip Carrier	5V	0 to 33	SOT187-2
OTP	P87C51UFA A					
ROM	P80C51UFPN	P80C31UFPN	-40 to +85, Plastic Dual In-line Package	5V	0 to 33	SOT129-1
OTP	P87C51UFPN					
ROM	P80C51UFBB	P80C31UFBB	-40 to +85, Plastic Quad Flat Pack	5V	0 to 33	SOT307-2
OTP	P87C51UFBB					

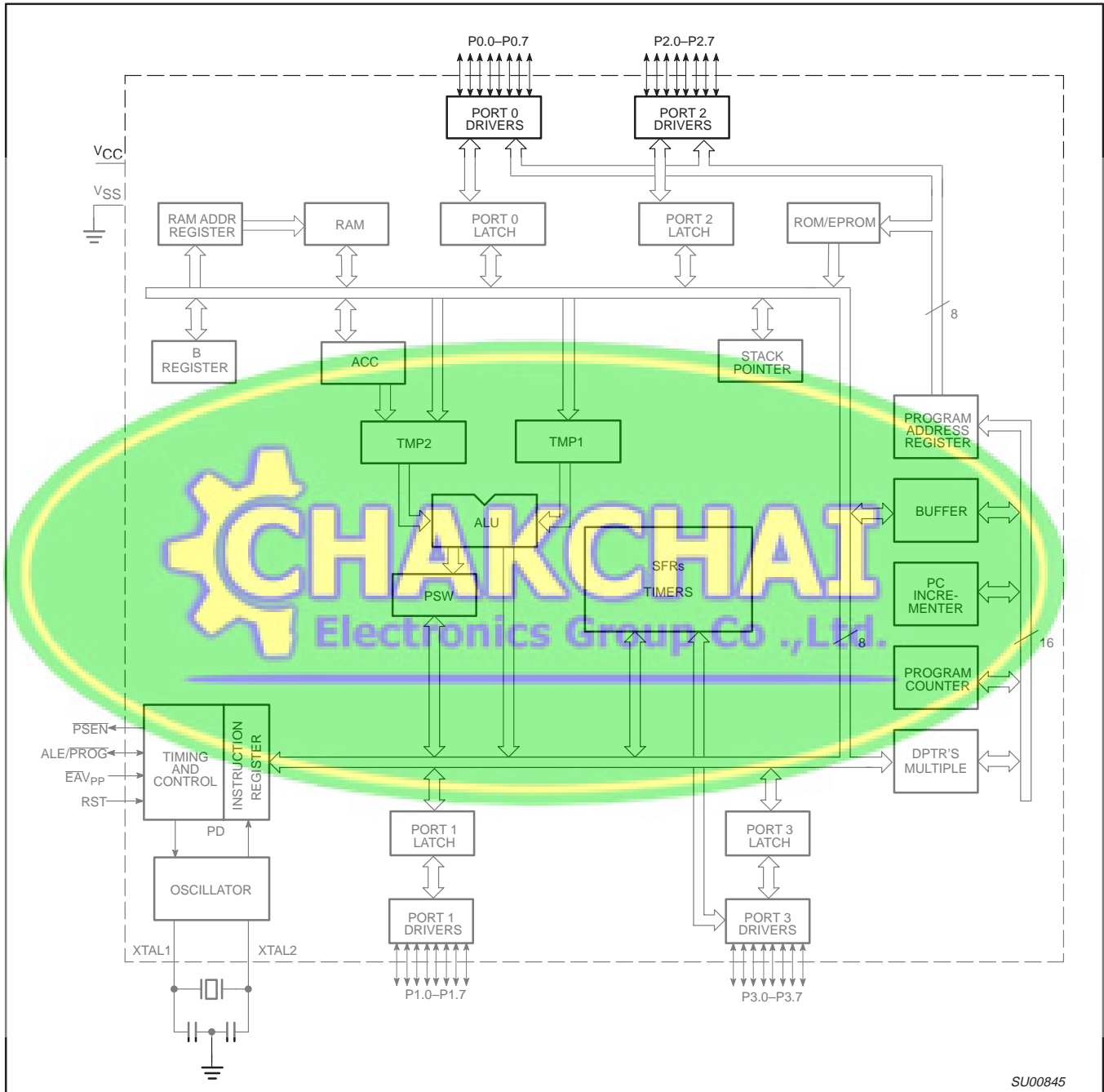
80C51/87C51 AND 80C31 ORDERING INFORMATION

DEVICE NUMBER (P87C51)	OPERATING FREQUENCY, MAX (S)	TEMPERATURE RANGE (B)	PACKAGE (AA)
P80C51 ROM	S = 16 MHz	B = 0° to +70°C	AA = PLCC
P87C51 OTP	U = 33 MHz	F = -40°C to +85°C	BB = PQFP
P80C31 ROMless			PN = PDIP

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BLOCK DIAGRAM

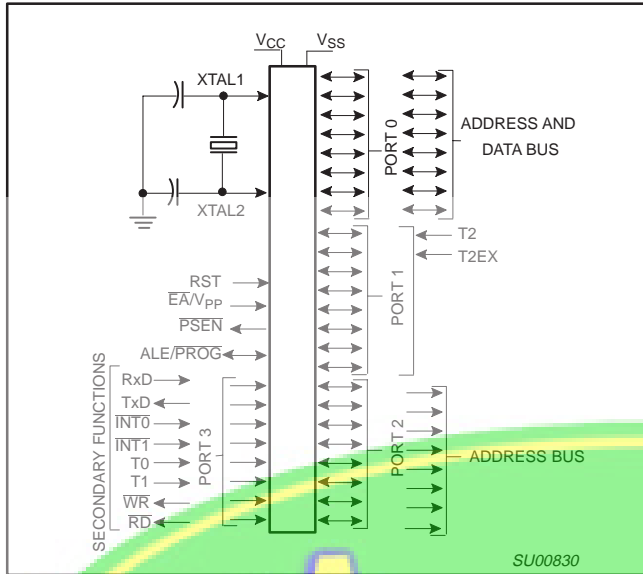


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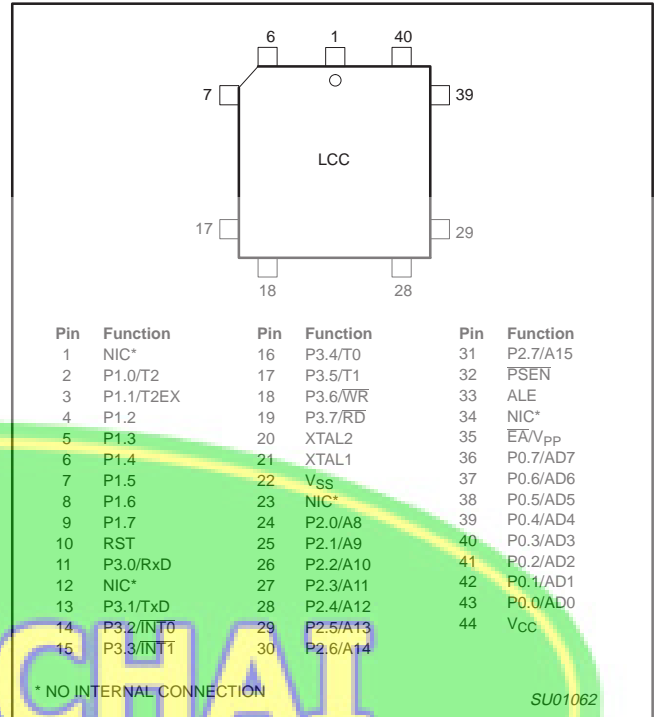
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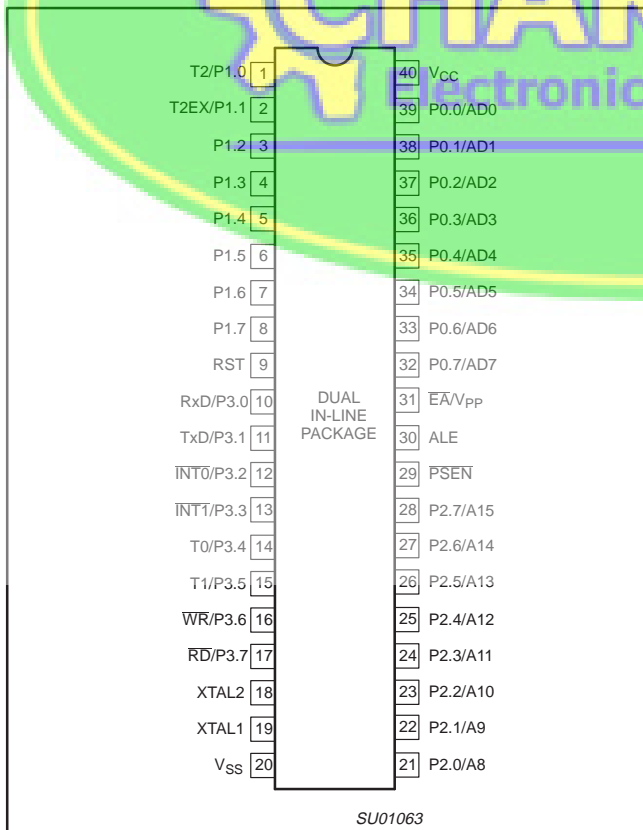
LOGIC SYMBOL



PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



PIN CONFIGURATIONS



PLASTIC QUAD FLAT PACK PIN FUNCTIONS

