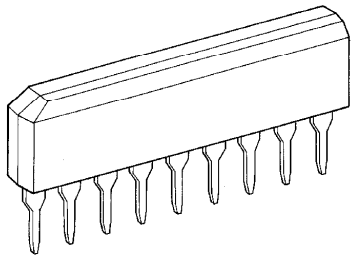
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA7900S, TA7900F

5V VOLTAGE REGULATOR WITH WATCHDOG TIMER

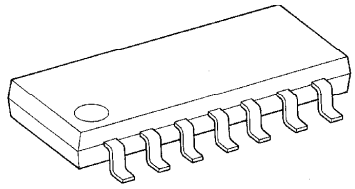
The TA7900S, TA7900F is an IC specially designed for micro-computer systems. It produces an output voltage of 5 ± 0.25V without need for adjustment from its accurate reference voltage and amplifier circuit.
At power-on, it outputs a reset signal to reset the system. It will also output a reset signal when the 5V output voltage drops below 92% because of external disturbance or other problem. It also incorporates a watchdog timer for self-diagnosing the system. When the system malfunctions, the IC generates reset pulses intermittently to prevent the system from running away.

TA7900S



SIP9-P-2.54A

TA7900F



SOP14-P-225-1.27

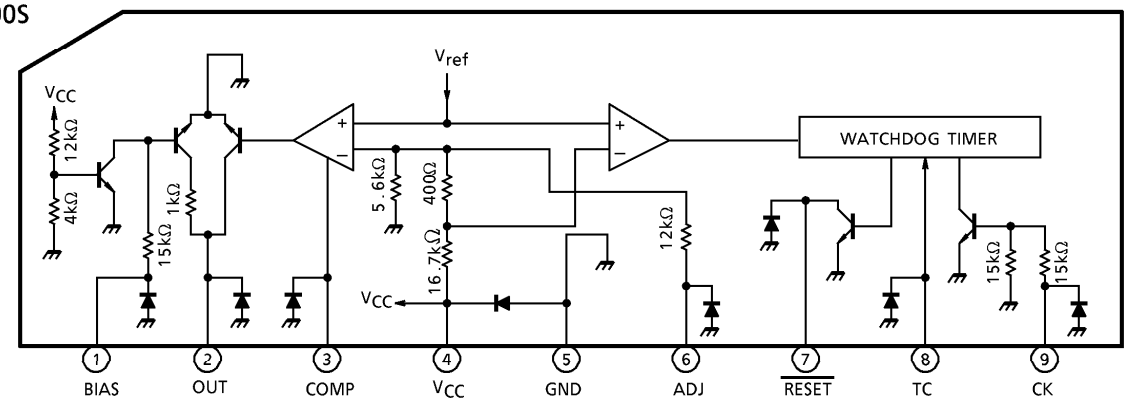
Weight
SIP9-P-2.54A : 0.92g (Typ.)
SOP14-P-225-1.27 : 0.2g (Typ.)

FEATURES

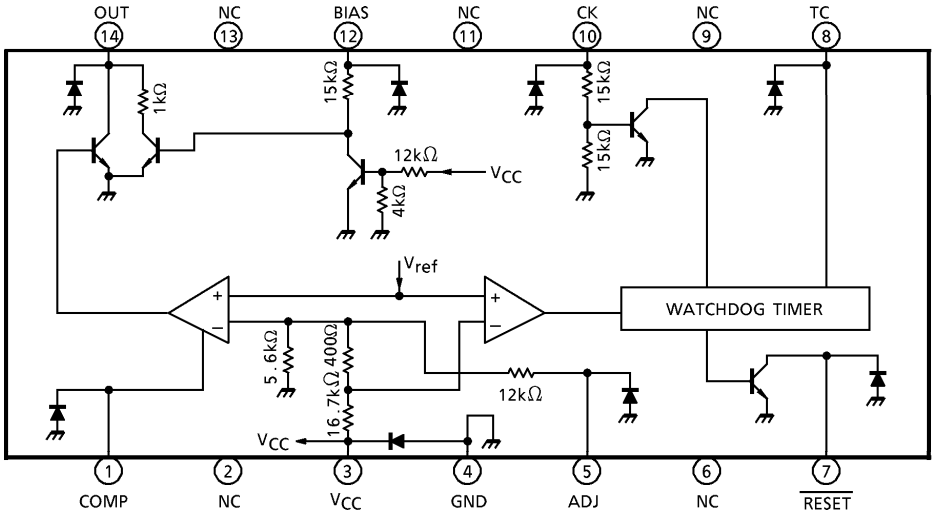
- Accurate output : 5 ± 0.25V
- Output voltage adjusting pin attached
- Power-on reset timer incorporated
- Watchdog timer incorporated
- Operating temperature range : from −40 to 85°C
- Wide operating voltage range : 40V (max.)
- Small SIP-9 pin (TA7900S)
- SOP-14 pin (TA7900F)

BLOCK DIAGRAM AND PIN LAYOUT

TA7900S



TA7900F



Note : The TA7900S and TA7900F are the same chip, except that they are housed in different packages.

PIN DESCRIPTION

PIN No.		SYMBOL	DESCRIPTION
TA7900S	TA7900F		
1	12	BIAS	Power supply starting pin. The starting current is supplied through a resistor to which the input voltage is applied. The output current from this starting current is as follows : I_{OUT} (BIAS PIN) $\geqq 30 \times (V_{IN} - 0.7) / (15 + R_1)$ (mA) where R_1 is the external resistance attached to BIAS pin (kΩ). When V_{CC} rises above 2.7V, the starting current is absorbed in the internal circuit ; instead, I_{OUT} is supplied via V_{CC}.
2	14	OUT	Connected to the base of an external PNP transistor so that the output voltage is stabilized. Power supply design suitable for particular load capacities is thus possible. Since the recommended maximum I_{OUT} is 5mA, an output current of 300mA is assured if the external transistor has an H_{FE} of 60 or more.
3	1	COMP	Phase compensation pin for output stabilization
4	3	V_{CC}	Power supply pin for internal circuit. The output voltage can also be detected at this pin.
5	4	GND	Grounded
6	5	ADJ	Output voltage adjust pin. The voltage can be raised by inserting a resistor between GND and this pin and can be lowered by inserting a resistor between V_{CC} and this pin. The voltage can be adjusted more or less ±1V in this way.
7	7	$\overline{\text{RESET}}$	NPN transistor open-collector output. (1) The signal goes low when the output drops below 92% of the specified level. (2) The pin supplies a reset signal determined by the CR combination connected to the TC pin. (3) The pin supplies reset pulses intermittently if no clock is given to the CK pin. This function is useful when the IC is used as a watchdog timer for a microcomputer system.
8	8	TC	This pin is used to set the time on the reset timer and watchdog timer. The time can be set using an external C_T and R_T.
9	10	CK	Input pin for watchdog timer. The pin is pulled up to V_{CC} if the IC is used only as a power-on reset timer.
—	2, 6, 9, 11, 13	NC	Not connected. (This pin electrically is completely open.)

Functional Description

The TA7900S / F contains a 5V constant-voltage power supply function to feed a stable power supply voltage to the CPU, etc., and a system reset function to ensure a stable operation of the CPU, etc. These functions are explained below.

(1) 5V constant-voltage power supply function

This function has a reference voltage Vref within the IC that is unaffected by temperature and input voltage changes. This voltage is stepped up to 5V by using an op-amp and dividing resistor. These op-amp and dividing resistor plus the output transistor connected to the op-amp's output configure a closed loop.
When using only the reset timer without using this power supply function, be sure to connect the BIAS OUT COMP pin to GND.

(2) System reset function (See the timing chart)

(2-1) Voltage monitoring function

If the voltage Vcc applied to the CPU exceeds 4.6V when powered on, the power-on reset timer starts from that point in time. If the Vcc drops below 4.6V when powered off, a reset signal is output immediately. Also, when the V_{CC} drops for some reason under normal operating condition, a reset signal is output immediately, and when the V_{CC} exceeds 4.6V after being restored to the normal voltage, the power-on reset timer starts from that point in time.

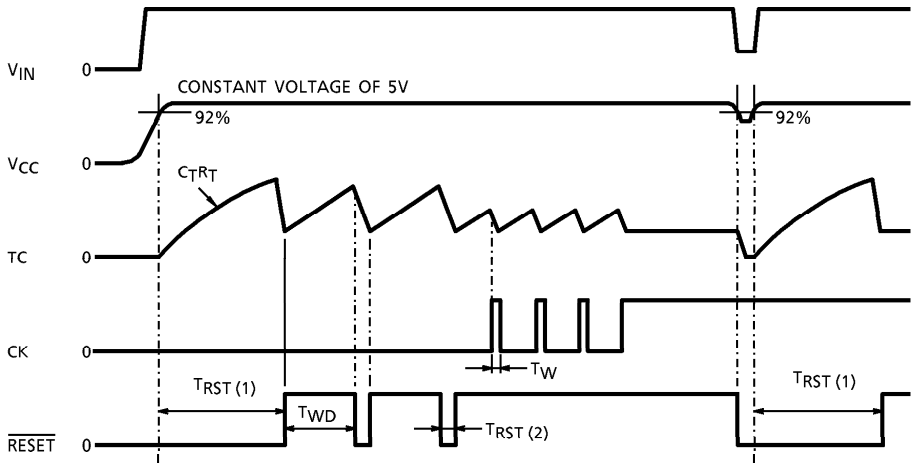
(2-2) Power-on reset timer function

The reset signal is deasserted after holding the device in a reset state for a predetermined time until the 5V constant voltage stabilizes at power-on time or until the oscillating clock fed to the CPU, etc. stabilizes. This duration of time can be set as desired by choosing the values of the external resistor and capacitor connected to the TC pin.
When the V_{CC} voltage exceeds 4.6V, current is sourced to start charging the capacitor and when this charge voltage exceeds 4V, the capacitor is discharged by the internal transistor. When the capacitor has been discharged to a voltage of 2V, the reset signal is inverted to deactivate the reset.

(2-3) Watchdog timer function

Program the CPU system software to output a clock each time one program routine is completed and enter this clock to the device's CK pin. Although the TC pin of the device repeatedly charges and discharges between 2V and 4V, when a clock pulse is applied, it switches to discharging in the middle of charging and starts charging from 2V again. Since when the CPU system is operating normally the clock is generated at predetermined intervals, the pin switches to discharging before the charge voltage reaches 4V. However, if no clock is applied while charging from 2V to 4V, it is assumed that the clock has been interrupted, i.e., the CPU system has gone wild, thus generating a reset signal to reset the CPU system.
The CPU system and the device's CK pin are connected with a differentiating circuit. This is to ensure that even in the event the CPU system goes wrong, the CK pin is always fed with a low-level clock regardless of whether the clock output has stopped in the high or low state. If the CK pin is fixed high, no reset signal is output, in which case only the power-on reset timer operates.

TIMING CHART



(Note) $T_{RST\ (1)}$, $T_{RST\ (2)}$, T_{WD}, T_W : See Attached Electrical Characteristics.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V_{IN1}	40	V
	V_{IN2}	− 0.3 to + 16	
Output Current	I_{OUT1}	10	mA
	I_{OUT2}	4	
Output Voltage	V_{OUT1}	40	V
	V_{OUT2}	16	
Power Dissipation	P_D	500 / 280	mW
Operating Temperature	T_{opr}	− 40 to 85	°C
Storage Temperature	T_{stg}	− 55 to 150	°C
Lead Temperature-time	T_{sol}	260 (10s)	°C

V_{IN1} : BIAS input
V_{IN2} : CK input
I_{OUT1}, V_{OUT1} : OUT output
I_{OUT2}, V_{OUT2} : $\overline{RESET}$ output
P_D : TA7900S / TA7900F

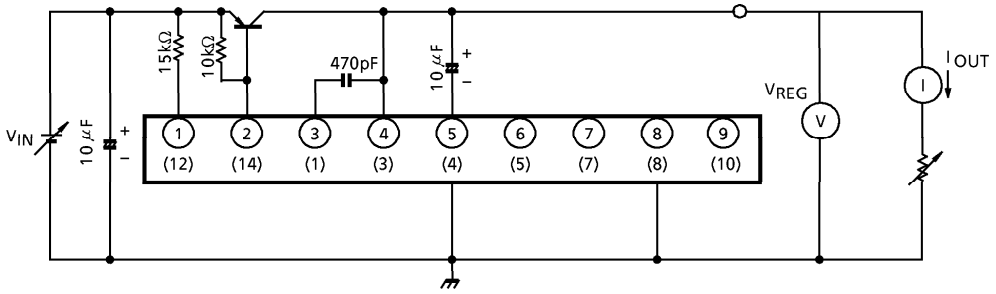
ELECTRICAL CHARACTERISTICS (V_{IN} = 7 to 17V, Ta = −40 to 85°C)

CHARACTERISTIC	SYMBOL	PIN	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{REG}	V_{CC}	1	—	4.75	5.0	5.25	V
Line Regulation	—	V_{CC}	—	V_{IN} = 7 to 40V	—	0.1	0.5	%
Load Regulation	—	V_{CC}	—	I_{LOAD} = 1 to 50mA	—	0.1	0.5	%
Temperature Coefficient	—	V_{CC}	—	—	—	0.01	—	% / °C
Output Voltage	V_{OL}	$\overline{RESET}$	2	I_{OL} = 2mA	—	—	0.5	V
Output Leakage Current	I_{LEAK}	$\overline{RESET}$	3	V_{OUT} = 10V	—	—	5	μA
Input Current	I_{IN}	TC	4	V_{IN} = 0 to 3.5V	−3	—	3	μA
Threshold Voltage	V_{IH}	TC	5	$\overline{RESET}$ "High" to "Low"	—	80% × V_{REG}	—	V
	V_{IL}			$\overline{RESET}$ "Low" to "High"	—	40% × V_{REG}	—	
Input Current	I_{IN}	CK	6	V_{IN} = 5V	—	0.3	0.7	mA
Input Voltage	V_{IH}	CK	5	—	2	—	—	V
	V_{IL}			—	—	—	0.5	
Reset Detect Voltage	—	V_{CC}	—	—	89% × V_{REG}	92% × V_{REG}	95% × V_{REG}	V
Standby Current	I_S	V_{CC}	8	V_{IN} = 14V	—	5	6.5	mA
Watchdog Timer	T_{WD}	$\overline{RESET}$	7	—	0.9 × C_TR_T	1.1 × C_TR_T	1.3 × C_TR_T	ms
Reset Timer (1)	$T_{RST\ (1)}$	$\overline{RESET}$	7	—	1.3 × C_TR_T	1.6 × C_TR_T	1.9 × C_TR_T	
Reset Timer (2)	$T_{RST\ (2)}$	$\overline{RESET}$	7	—	0.15 × C_T	0.3 × C_T	0.6 × C_T	
Clock Pulse Width	T_W	CK	—	—	3	—	—	μs

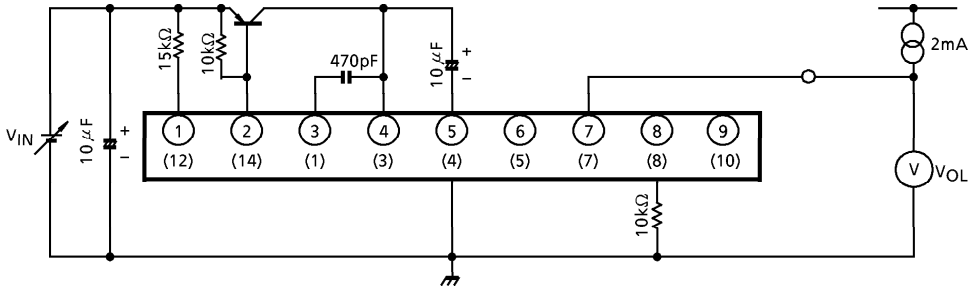
Note : Reset timer (1) : Power-on reset time
Reset timer (2) : Watchdog reset time
The unit of C_T is μF : the unit of R_T is kΩ.

TEST CIRCUIT (Circles O indicate the pin numbers on the TA7900S or TA7900F.)

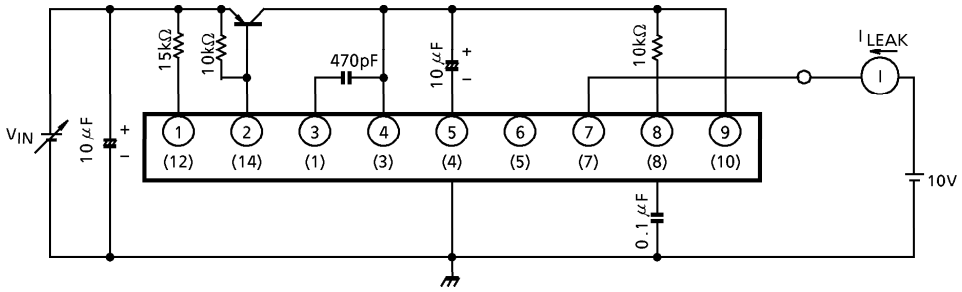
1. V_{REG}



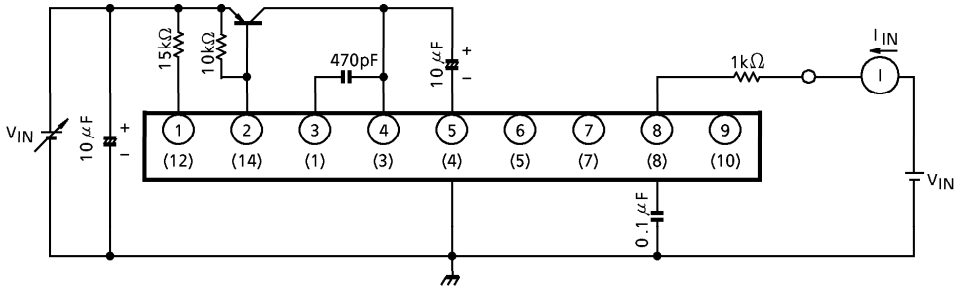
2. V_{OL} ($\overline{RESET}$)



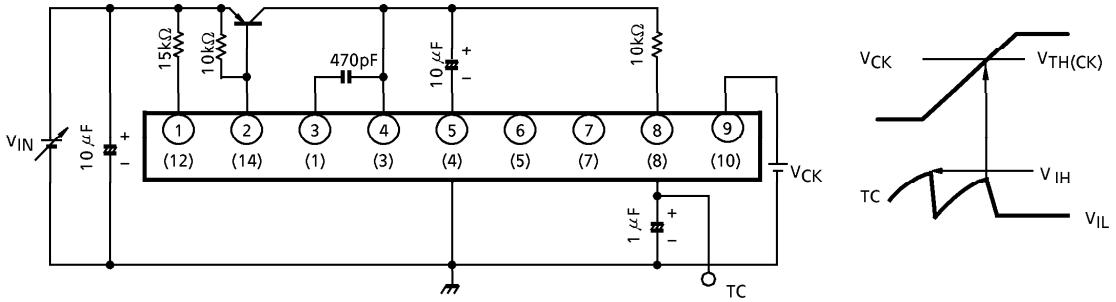
3. I_{LEAK} ($\overline{RESET}$)



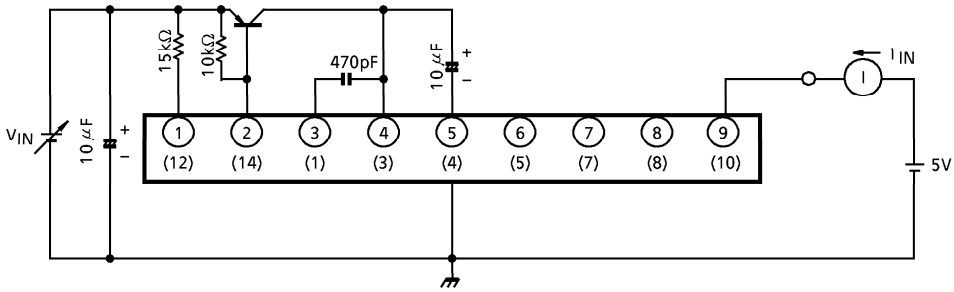
4. I_{IN} (TC)



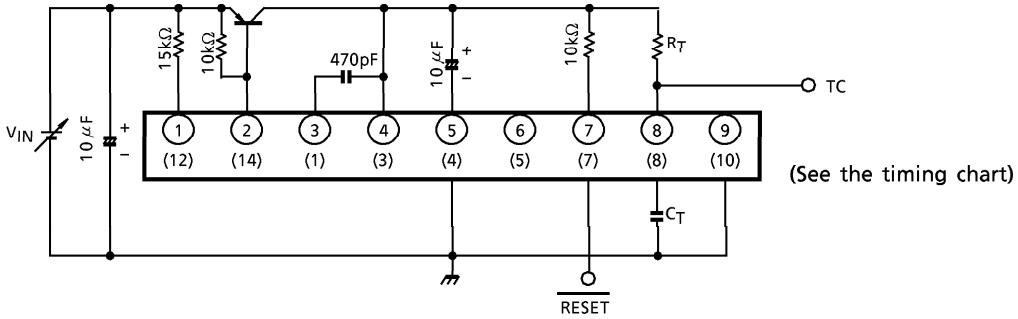
5. V_{IH}、 $V_{IL\,(TC)}$、V_{IH}、$V_{IL\,(CK)}$



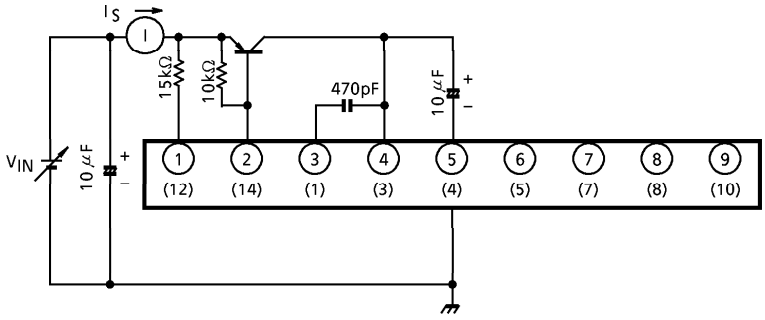
6. $I_{IN\,(CK)}$



7. V_{RESET}、T_{WD}、$T_{RST\,(1)}$、$T_{RST\,(2)}$

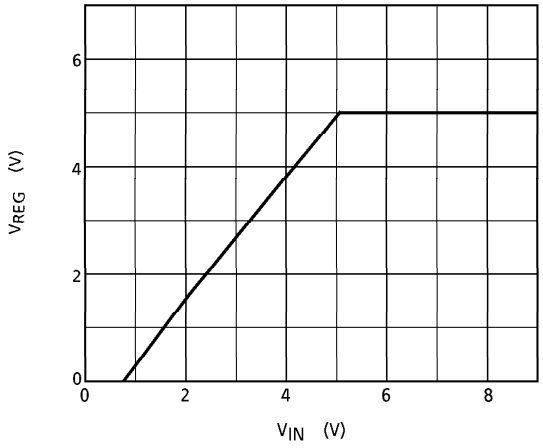


8. I_S

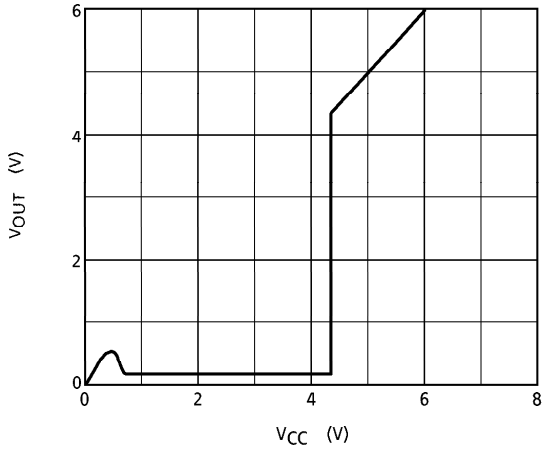


TYPICAL CHARACTERISTICS

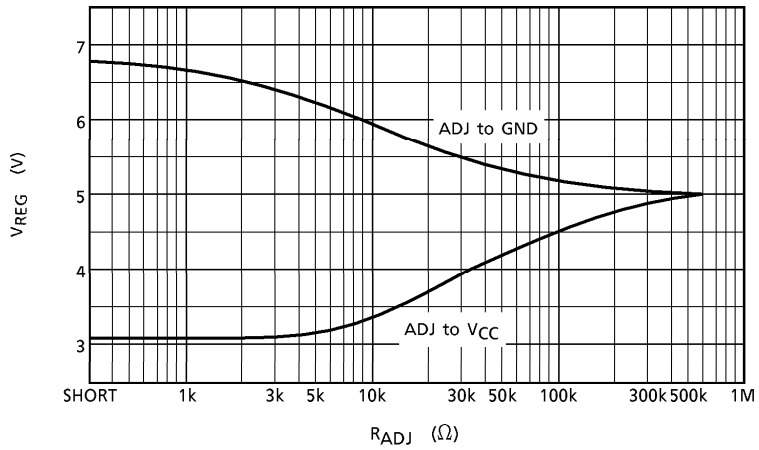
1. Input-output characteristic
($R_L = 25\Omega$, external transistor 2SA968-Y)
(R_L: Load resistance between Vreg and GND)



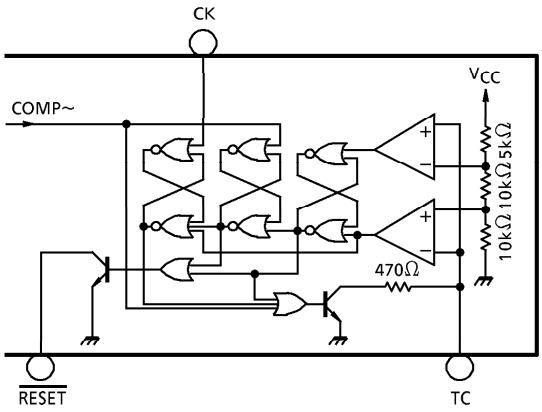
2. Reset Output Characteristic



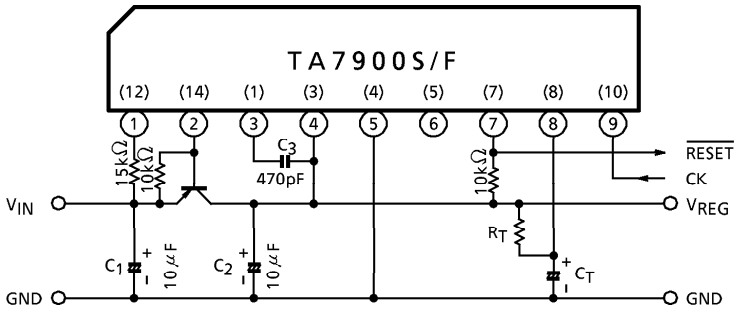
3. Output Adjusting Resistance Characteristic



RESET TIMER EQUIVALENT CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT (Circles O indicate the pin numbers on the TA7900S or TA7900F.)



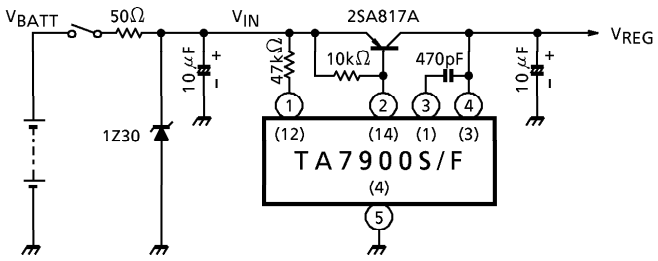
* Cautions for Wiring

1. C_1 and C_2 are for absorbing disturbance, noise, etc. Connect them as close to the IC as possible.
2. C_3 is for phase compensation. Also, connect C_3 close to the IC.

120 Vpeak (200ms) LOAD DUMP

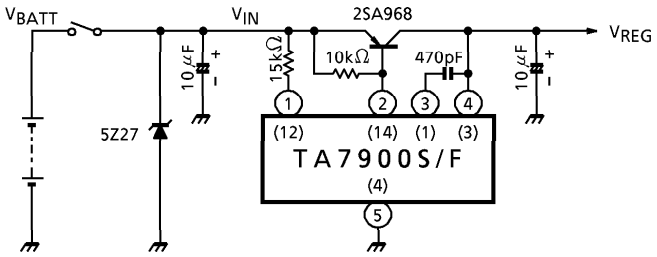
1. Low Output Current Circuit

   I_{LOAD} = 10mA Max., V_{BATT} = 6 to 17V

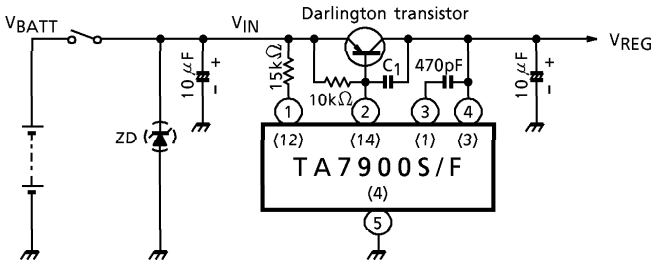


2. High Output Current Circuit

I_{LOAD} = 300mA Max., V_{BATT} = 6~17V



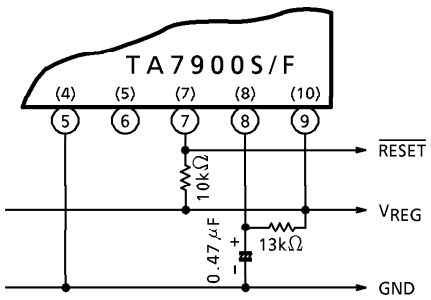
EXAMPLE OF APPLICATION CIRCUIT USING DARLINGTON TRANSISTOR



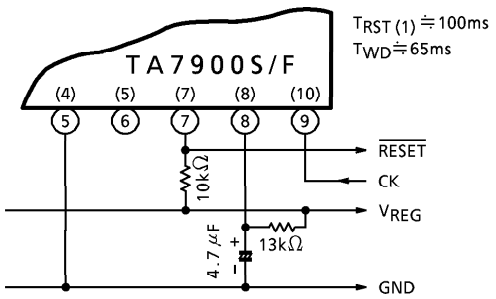
* Select a C_1 value according to the working condition -- typically above 2000pF. Insert ZD when necessary.

APPLICATION CIRCUIT OF WATCHDOG / RESET TIMER

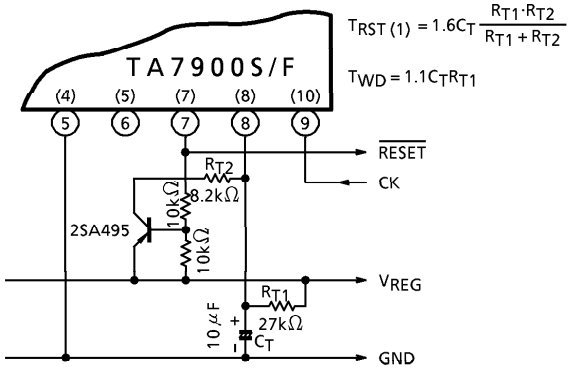
1. $T_{RST\,(1)} \fallingdotseq 10ms$ ····· Power-On Reset Timer



2. $T_{RST\,(1)} \fallingdotseq 1.5T_{WD}$



3. $T_{RST\,(1)} \fallingdotseq 100ms$, $T_{WD} \fallingdotseq 300ms$



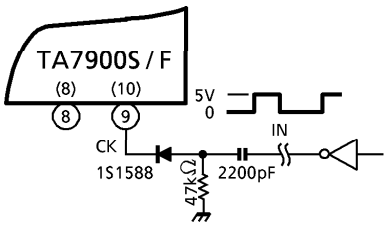
4. Recommended Conditions

PART NAME	MIN.	MAX.	UNIT
C_T	0.01	100	μF
R_T	5	100	kΩ
R_{T1}	—	100	kΩ
R_{T1} // R_{T2} (Note)	5	—	kΩ

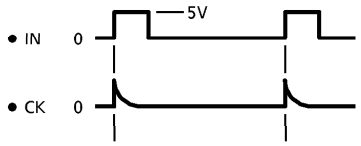
(Note) $R_{T1} // R_{T2} = (R_{T1} \times R_{T2}) / (R_{T1} + R_{T2})$

CK INPUT APPLICATION CIRCUIT

○ Capacitor Coupling



○ Timing Chart

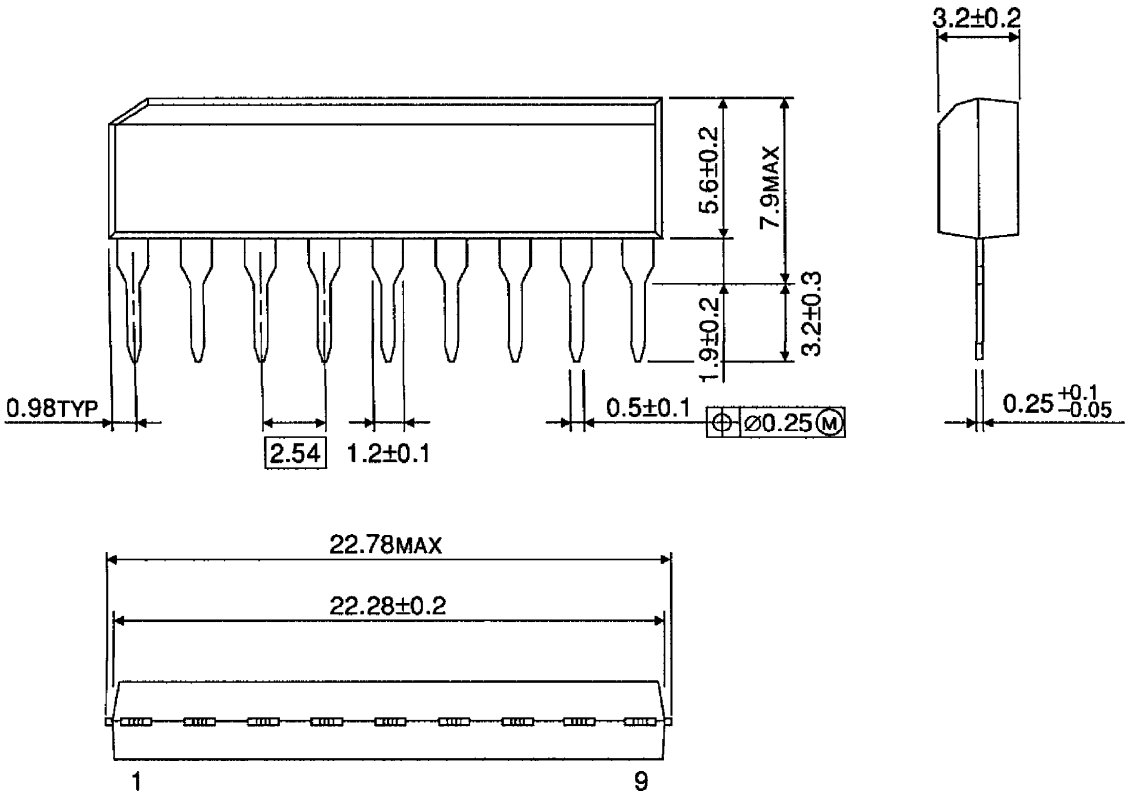


The capacitor coupling allows reset pulses to be supplied intermittently from the $\overline{RESET}$ pin whether the input level (IN) is high or low.

OUTLINE DRAWING

SIP9-P-2.54A

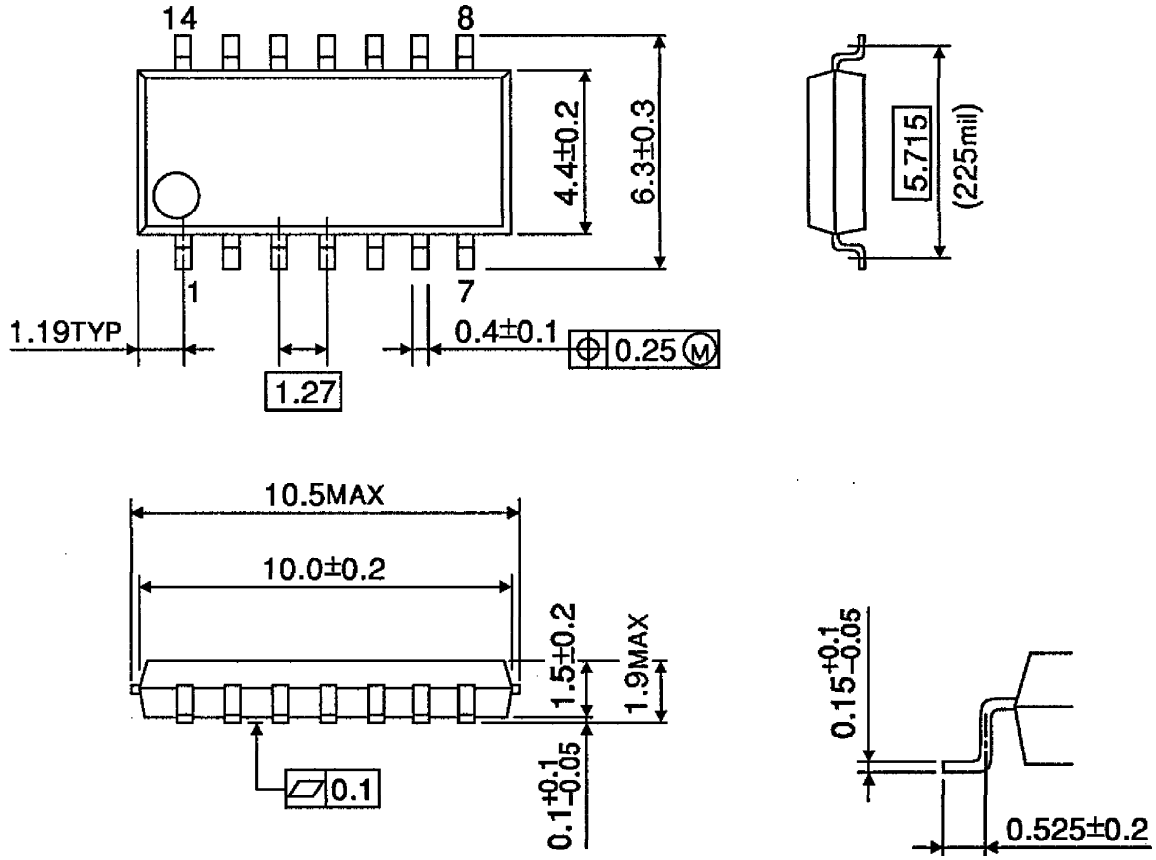
Unit : mm



Weight : 0.92g (Typ.)

OUTLINE DRAWING

SOP14-P-225-1.27 Unit : mm



Weight : 0.2g (Typ.)