Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family

- Precision Reference Internally Trimmed to ±1%

- High-Performance Current Limit Function

- Under-Voltage Lockout with Hysteretic Turn-on

- Start-Up Supply Current Less Than 4mA

- Output Current to 200mA

- 60V Output Capability

- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers

- PWM Latch Insures Single Pulse per Period

- Double Pulse Suppression Logic

- 200ns Shutdown through PWM Latch

- Ensured Frequency Accuracy

- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to +125°C. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -40°C to +85°C and 0°C to 70°C, respectively. Surface mount devices are also available.
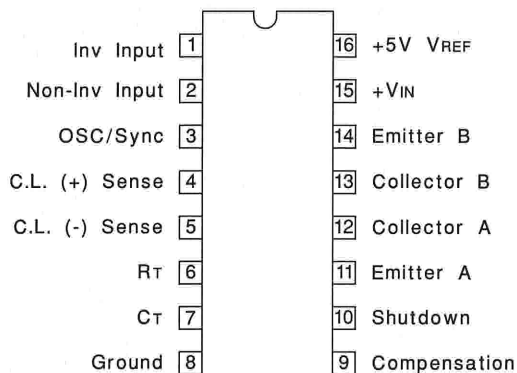
BLOCK DIAGRAM
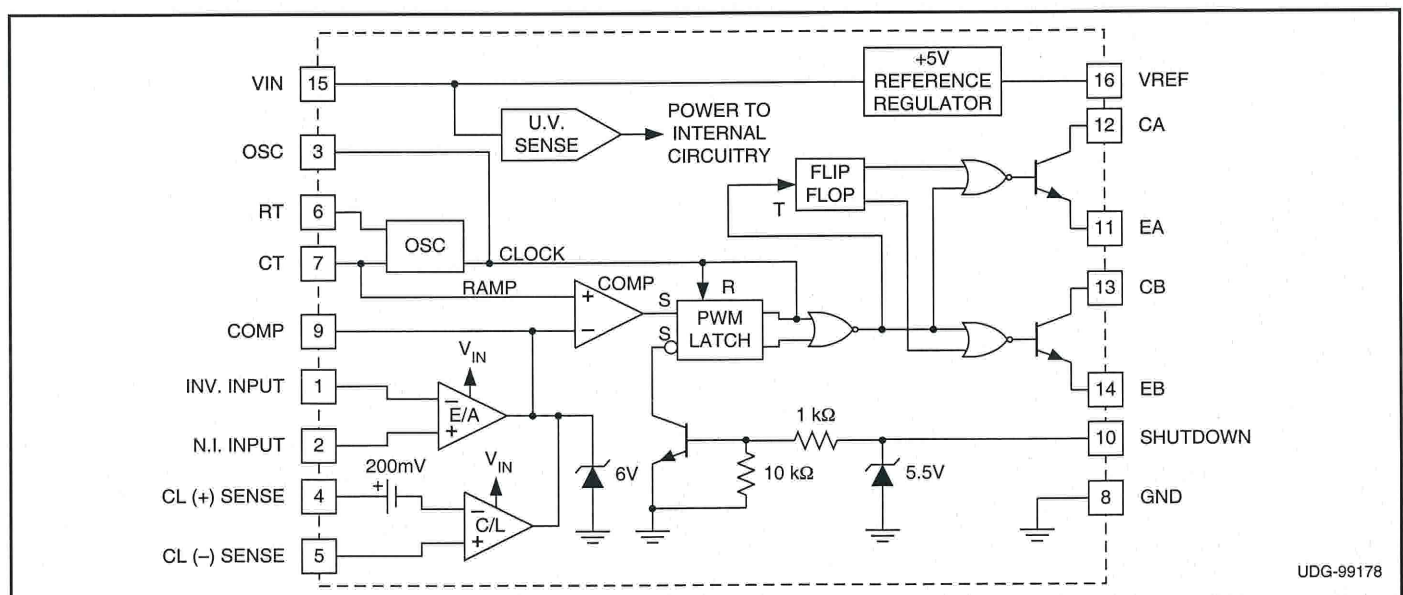
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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 60V
Output Current (each Output) 200mA
Maximum Forced Voltage (Pin 9, 10) . . . . -3 to +5V
Maximum Forced Current (Pin 9, 10) . . . . ±10mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Temperature Range . . . . -55°C to +125°C
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature, (Soldering, 10 seconds) . . . . +300°C
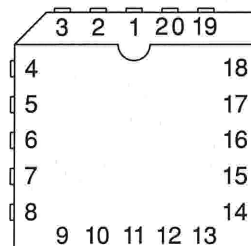*Note: Consult packaging section of Databook for thermal limitations and considerations of package.*

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package

Inv Input [1]	[16] +5V V_{REF}
Non-Inv Input [2]	[15] +V_{IN}
OSC/Sync [3]	[14] Emitter B
C.L. (+) Sense [4]	[13] Collector B
C.L. (-) Sense [5]	[12] Collector A
R_T [6]	[11] Emitter A
C_T [7]	[10] Shutdown
Ground [8]	[9] Compensation

CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q or L Package

Pins: 3 2 1 20 19 (top), 4, 5, 6, 7, 8 (left side), 18, 17, 16, 15, 14 (right side), 9 10 11 12 13 (bottom)

PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
R_T	8
C_T	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+V_{IN}	19
+5V V_{REF}	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V_{REF} = 0, 25°C ≤ T_J ≤125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T_J =25°C		40			40		µVrms
Long Term Stability*	T_J =125°C, 1000 Hrs.		20	50		20	50	mV

* These parameters are ensured by design but not 100% tested in production.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	µs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_J = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	µA
Input Offset Current			.05	1		0.5	1	µA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔV_O= 1 to 4V, $R_L \geq$ 10MΩ	72	80		64	80		dB
Gain-Bandwidth*	T_J = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*§	T_J = 25°C, 30kΩ $\leq R_L \leq$ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 2kΩ, C_T = 0.01mfd)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_J = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	µA
Common Mode Rejection Ratio	V(pin 5) = -0.3V to + 5.5V	50	60		50	60		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10MΩ	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100µA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	µA

* These parameters are ensured by design but not 100% tested in production.
§ DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: A_V = $g_M R_L$ where R_L is the resistance from pin 9 to the common mode voltage.
The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.
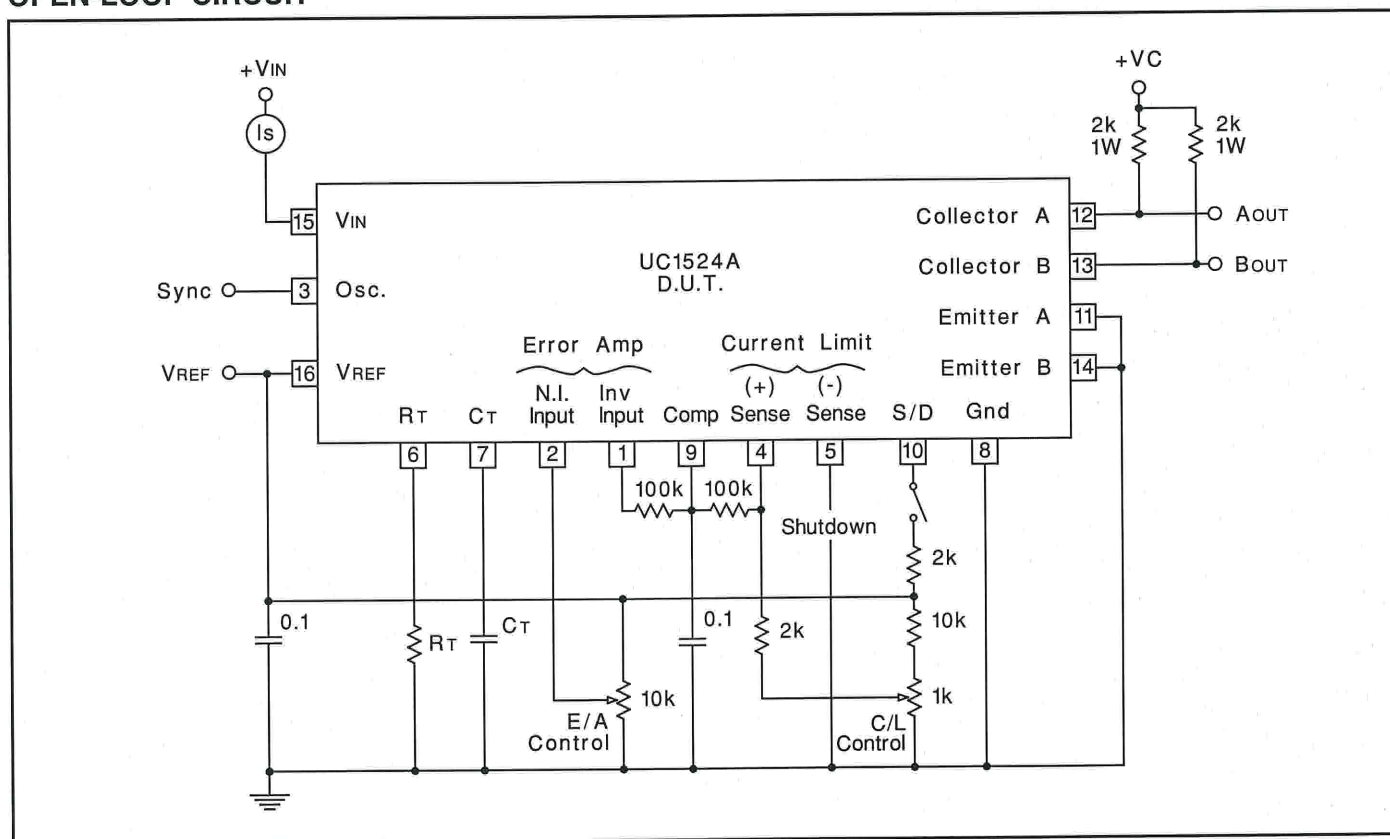Note 1: Min Limit applies to output high level, max limit applies to output low level.
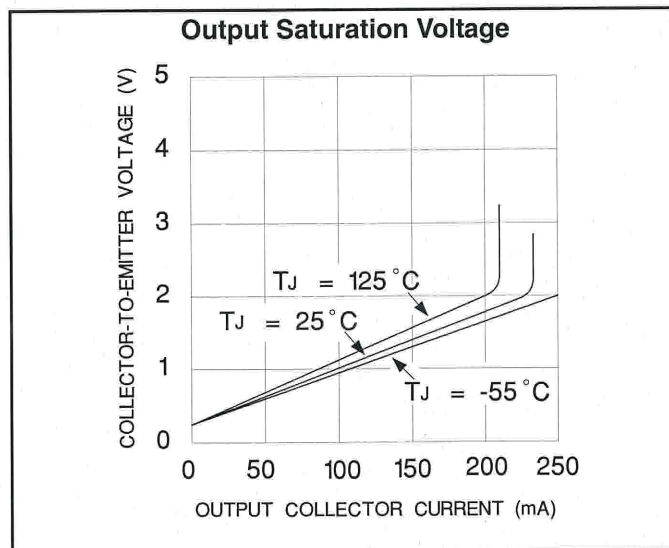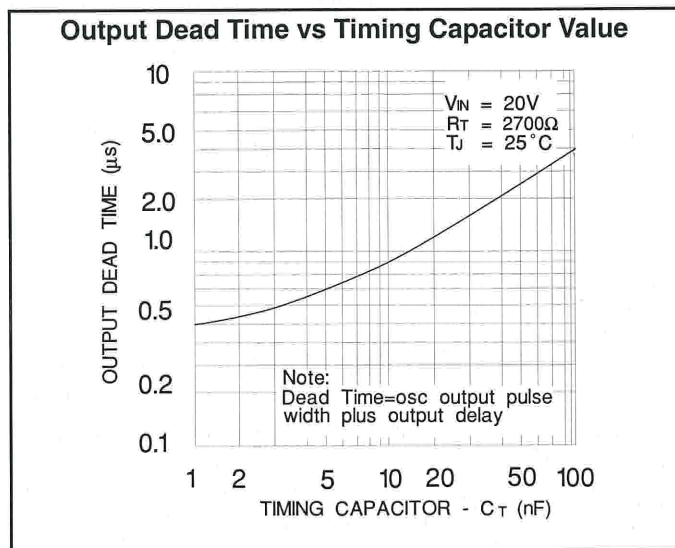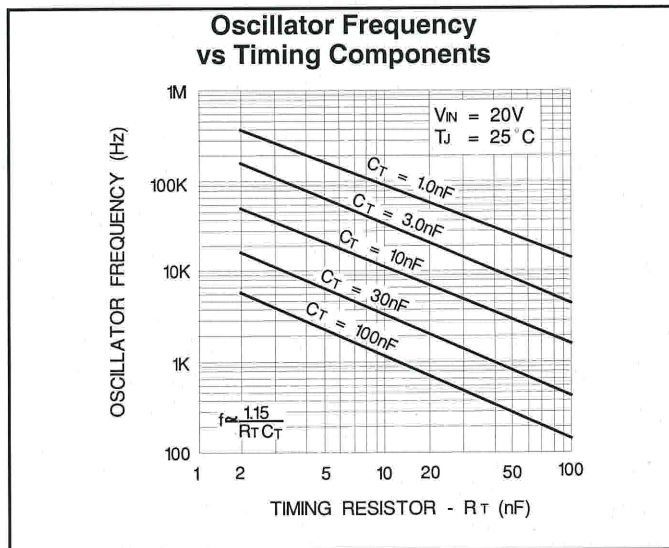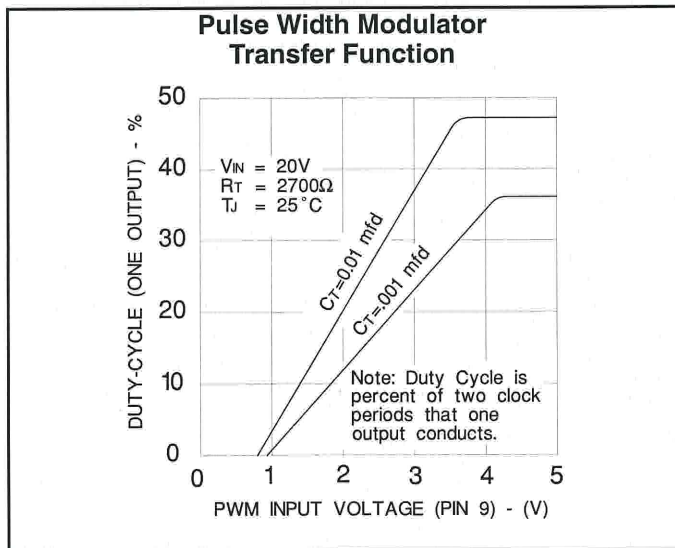
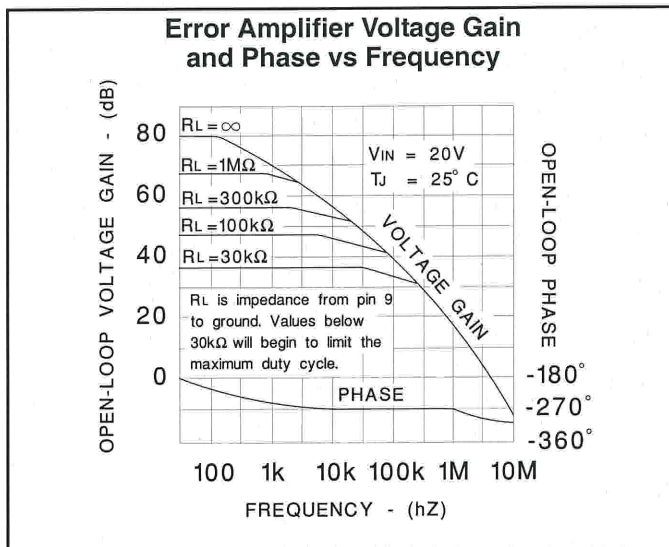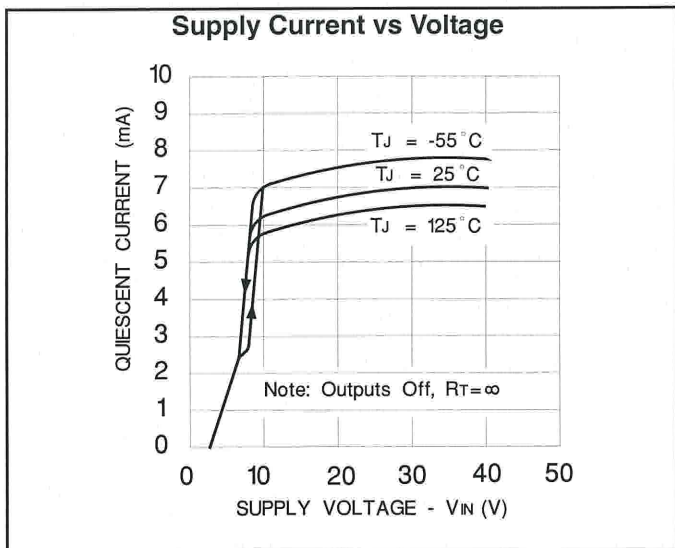**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -40° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.) (Each Output)								
Saturation Voltage	I_C = 20mA		.2	.4		.2	.4	V
	I_C = 200mA		1	2.2		1	2.2	V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_J = 25°C, R = 2kΩ		120	400		120	400	ns
Fall Time*	T_J = 25°C, R = 2kΩ		25	200		25	200	ns
Comparator Delay*	T_J = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_J = 25°C, Pin 10 to output		200			200		ns
Shutdown Threshold	T_J = 25°C, R_C = 2kΩ	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

These parameters are ensured by design but not 100% tested in production.

OPEN-LOOP CIRCUIT

Supply Current vs Voltage

QUIESCENT CURRENT (mA)

$T_J = -55°C$
$T_J = 25°C$
$T_J = 125°C$

Note: Outputs Off, $R_T = \infty$

SUPPLY VOLTAGE - V_{IN} (V)

Error Amplifier Voltage Gain and Phase vs Frequency

OPEN-LOOP VOLTAGE GAIN - (dB)

OPEN-LOOP PHASE

$R_L = \infty$
$R_L = 1M\Omega$
$R_L = 300k\Omega$
$R_L = 100k\Omega$
$R_L = 30k\Omega$

$V_{IN} = 20V$
$T_J = 25°C$

VOLTAGE GAIN

R_L is impedance from pin 9 to ground. Values below $30k\Omega$ will begin to limit the maximum duty cycle.

PHASE

-180°
-270°
-360°

FREQUENCY - (hZ)

Pulse Width Modulator Transfer Function

DUTY-CYCLE (ONE OUTPUT) - %

$V_{IN} = 20V$
$R_T = 2700\Omega$
$T_J = 25°C$

$C_T = 0.01$ mfd
$C_T = .001$ mfd

Note: Duty Cycle is percent of two clock periods that one output conducts.

PWM INPUT VOLTAGE (PIN 9) - (V)

Oscillator Frequency vs Timing Components

OSCILLATOR FREQUENCY (Hz)

$V_{IN} = 20V$
$T_J = 25°C$

$C_T = 1.0nF$
$C_T = 3.0nF$
$C_T = 10nF$
$C_T = 30nF$
$C_T = 100nF$

$f \approx \dfrac{1.15}{R_T C_T}$

TIMING RESISTOR - R_T (nF)

Output Dead Time vs Timing Capacitor Value

OUTPUT DEAD TIME (µs)

$V_{IN} = 20V$
$R_T = 2700\Omega$
$T_J = 25°C$

Note:
Dead Time=osc output pulse width plus output delay

TIMING CAPACITOR - C_T (nF)

Output Saturation Voltage

COLLECTOR-TO-EMITTER VOLTAGE (V)

$T_J = 125°C$
$T_J = 25°C$
$T_J = -55°C$

OUTPUT COLLECTOR CURRENT (mA)

Current Limit Amplifier Delay

Output At Pin 9

Overdrive
- 5%
- 10%
- 20%
- 50%

OUTPUT (V): 6 5 4 3 2 1 0

INPUT (V): 0.2 0.1 0

Input At Pin 4

$V_{IN} = 20v$, $T_J = 25°C$
Pin 2 Tied To Pin 16
Pin 5 Grounded

DELAY TIME (μs): 0 1 2 3 4

Shutdown Delay From PWM Comparator - Pin 9

OUTPUT (V): 20 15 10 5 0

$V_{IN} = 20V$
$R_L = 2k\Omega$
$T_J = 25°C$

Output At
Pin 12 OR 13

INPUT (V): 5 4 3 2 1 0

Input At Pin 9

Note: Minimum input pulse width to latch is 200ns

DELAY TIME (μs): 0 1 2 3
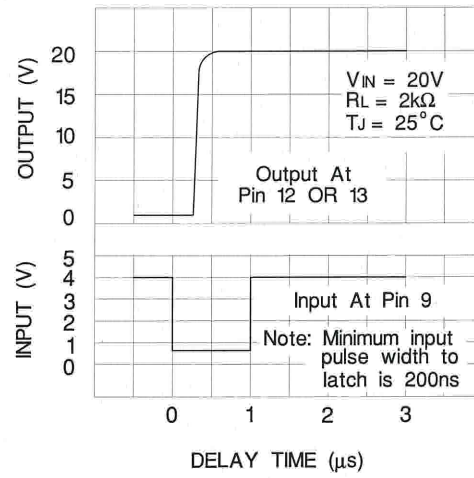
Turn-Off Delay From Shutdown - Pin 10

OUTPUT (V): 20 15 10 5 0

$V_{IN} = 20V$
$R_L = 2k\Omega$
$T_J = 25°C$

Output At
Pin 12 or 13

INPUT (V): 1.0 0.5 0

Input at Pin 10

Note: Minimum input pulse width to latch is 200ns

DELAY TIME (μs): 0 1 2 3
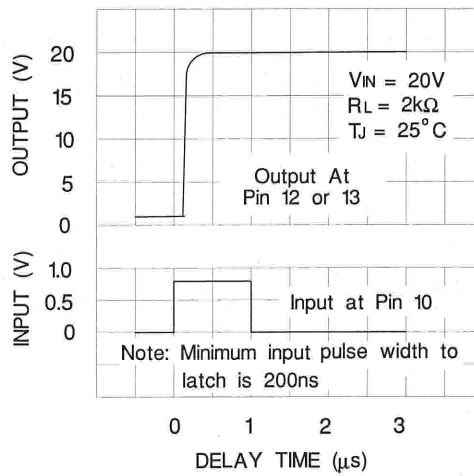
TEXAS INSTRUMENTS

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JOB NUMBER LOG

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2701036	UC1524A, UC2524A, UC3524A	SLUS181B	Papermaster, Barry	Albert, Rich	Revised	TIS-HPA	13-APR-2007		Update

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-8764502EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1524AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1524AJ883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC1524AL	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1524AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2524ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524ADWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2524AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC2524AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2524ANG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3524ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524ADWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3524AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
UC3524AN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3524ANG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2524ADWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3524ADWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2524ADWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3524ADWTR	SOIC	DW	16	2000	346.0	346.0	33.0

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package can be hermetically sealed with a metal lid.
         D. The terminals are gold plated.
         E. Falls within JEDEC MS-004

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package is hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

DW (R−PDSO−G16)   PLASTIC SMALL−OUTLINE PACKAGE

0.413 (10,50)
0.398 (10,10)

16   9

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
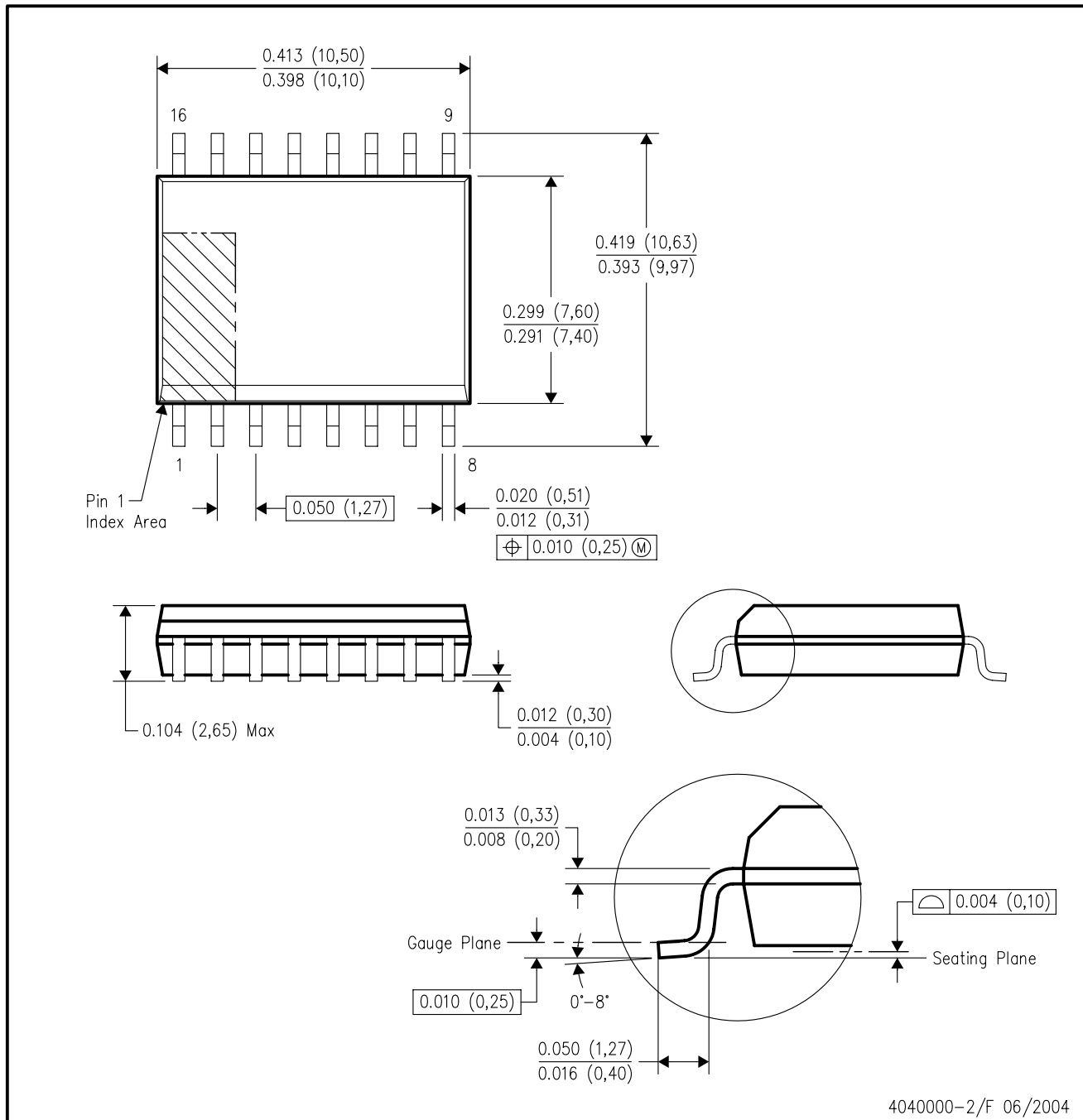
4040000−2/F 06/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AA.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

△C

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
B.   This drawing is subject to change without notice.
△C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
△D   The 20 pin end lead shoulder width is a vendor option, either half or full width.